PJ20030

5.5V, 300mA, Ultra Low Noise And Low Iq LDO In a Tiny Package

GENERAL DESCRIPTION

The PJ20030 series is a high-accuracy, low-noise, high-speed, high-PSRR, and low-dropout CMOS linear regulator with high ripple rejection. The devices offer a new level of cost-effective performance in cellular phones, laptop and notebook computers, and other portable devices.

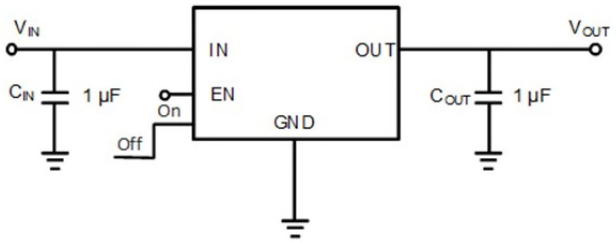
The PJ20030 has the fold-back maximum output current that depends on the output voltage. So the current limit functions both as a short-circuit protection and as an output current limiter.

The device is available in DFN1x1-4, SOT23-5, DFN0.8x0.8-4, and DFN2x2-6 packages.

FEATURES

- Operating input voltage range : 1.6 V to 5.5 V
- Output voltage range : 0.8 V to 3.3 V
- Output current : 300 mA
- Ultra-low quiescent current : 25 µA typ.
- Dropout voltage : 170 mV at IOUT = 300 mA
- PSRR: 75 dB at 1 kHz, IOUT = 20 mA
- Output voltage tolerance : ±1%
- Stable with ceramic capacitors 1 µF
- Thermal-overload protection
- Short-circuit protection
- Quick output discharge :
  - PJ20030A: With output discharge
  - PJ20030B: Without output discharge
- Available in small DFN1x1-4, SOT23-5, DFN0.8x0.8-4, and DFN2x2-6 packages
- These devices are Pb−Free, halogen Free/BFR free, and are RoHS compliant

SIMPLIFIED SCHEMATIC



APPLICATIONS

- MP3/MP4 players
- Cellphones, radiophones, digital cameras
- Bluetooth, wireless handsets
- Others portable electronics devices

ORDERING INFORMATION

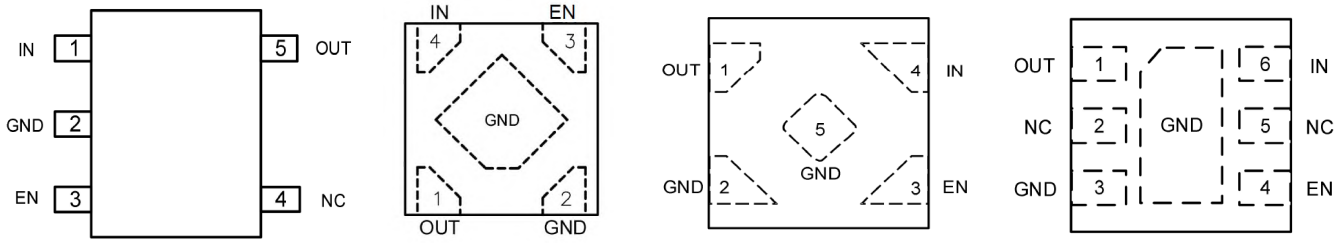
ORDER NUMBER	Marking ID	Package	Description
PJ20030A-xxS5_R1	AAADNN	SOT23-5	Halogen Free in T&R, 3000 pcs/Reel
PJ20030A-xxQZ1_R1	A W	DFN1x1-4	Halogen Free in T&R, 10000 pcs/Reel
PJ20030A-xxQZ_R1	A W	DFN0.8x0.8-4	Halogen Free in T&R, 5000 pcs/Reel
PJ20030A-xxQW_R1	AAAC	DFN2x2-6	Halogen Free in T&R, 3000 pcs/Reel
PJ20030B-xxS5_R1	AABDNN	SOT23-5	Halogen Free in T&R, 3000 pcs/Reel
PJ20030B-xxQZ1_R1	A W	DFN1x1-4	Halogen Free in T&R, 10000 pcs/Reel
PJ20030B-xxQZ_R1	A W	DFN0.8x0.8-4	Halogen Free in T&R, 5000 pcs/Reel
PJ20030B-xxQW_R1	AABC	DFN2x2-6	Halogen Free in T&R, 3000 pcs/Reel

Output Voltage Options											
Option Code “xx”	08	09	10	11	12	15	18	25	28	30	33
Voltage	0.8 V	0.9 V	1.0 V	1.1 V	1.2 V	1.5 V	1.8 V	2.5 V	2.8 V	3.0 V	3.3 V

Marking Information

Marking	Package	Definition
AABDNN	SOT23-5	AA: Product code B: Version D: Day code NN: Serial No
A W	DFN1x1-4 / DFN0.8x0.8-4	A: Product code W: Week code
AABC	DFN2x2-6	AA: Product code B: Version C: Week code

PIN CONFIGURATION



SOT23-5 **DFN1x1-4** **DFN0.8x0.8-4** **DFN2x2-6**

Pin Assignment (Top View)

FUNCTIONAL PIN DESCRIPTION

TERMINAL NAME	I/O(1)	DESCRIPTION
OUT	O/P	**Output voltage pin.**
EN	I	**Enable pin.** This pin has a 100 nA pull-down current source. Connect to logic “High” for normal operation.
GND	G	**Power supply ground.**
IN	I/P	**Input voltage pin.**
NC	G	**No connection**.

(1) I – Input; O – Output; P – Power; G – Ground

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN	-0.3	6.5	V
	VOUT, EN	-0.3	V_{IN}	V
I_{OUT}	Output Current	300		mA
T_L	Lead temperature range	260		°C
T_J(2)	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	1.6		5.5	V
T_J	Operating junction temperature	-40		125	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance, SOT23-5		235		°C/W
	Junction-to-ambient thermal resistance, DFN1x1-4		250		°C/W
	Junction-to-ambient thermal resistance, DFN0.8x0.8-4		400		°C/W
	Junction-to-ambient thermal resistance, DFN2x2-6		80		°C/W

ELECTRICAL CHARACTERISTICS

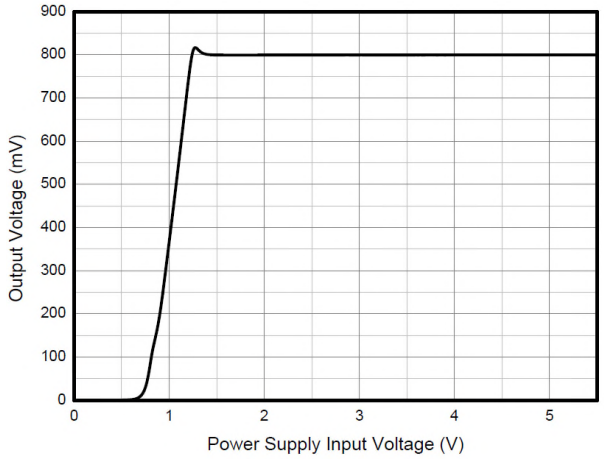
V_{IN} = V_{OUT} + 1 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0μF, T_A = -40°C to 125°C. Typical value is tested at T_J = +25°C, unless otherwise noted.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{IN}	Input voltage			1.6		5.5	V
V_{OUT}(1)	Output voltage			0.8		3.3	V
	Output accuracy	V_{OUT} < 2 V, T_A = 25°C		-20		20	mV
		V_{OUT} ≥ 2 V, T_A = 25°C		-1%		1%	V
I_{LIM}	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$			480		mA
V_{DO}	Dropout voltage	V_{OUT} = 0.95 x $V_{OUT(NOM)}$, I_{OUT} = 300 mA	$V_{OUT(NOM)}$ = 0.8V		950		mV
			$V_{OUT(NOM)}$ = 1.2V		650		
			$V_{OUT(NOM)}$ = 1.8V		280		
			$V_{OUT(NOM)}$ = 2.5V		200		
			$V_{OUT(NOM)}$ = 2.8V		170		
			$V_{OUT(NOM)}$ = 3.0V		160		
			$V_{OUT(NOM)}$ = 3.3V		150		
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	Line regulation	($V_{OUT(NOM)}$ + 1.0 V) ≤ V_{IN} ≤ 5.5 V			0.02		%/V
$\triangle V_{OUT}$	Load regulation	I_{OUT} = 0 mA to 350 mA, T_A = +25°C				40	mV
I_Q	Quiescent current	No load			25		μA
I_{SC}	Short circuit current	V_{OUT} = 0 V			220		mA
I_{SHDN}	Shut-down current	V_{EN} = 0 V, V_{IN} = 5.5 V			0.1		μA
PSRR	Power supply rejection rate	I_{OUT} = 20 mA	f = 100 Hz		80		dB
			f = 1 kHz		75		dB
			f = 10 kHz		70		dB
			f = 100 kHz		60		dB
			f = 1 MHz		45		dB
V_{IH}	EN pin threshold voltage	EN logic high voltage		1			V
V_{IL}		EN logic low voltage				0.4	V

I_{EN}	EN pull-down current	V_{EN} = 5.5 V			0.1		μA
e_n	Output voltage noise	f = 10 Hz to 100 kHz, V_{OUT} = 1.8 V, I_{OUT} = 1 mA			50		μV_{RMS}
T_{SD}	Thermal shutdown threshold	Shutdown, temperature increasing	I_{OUT} = 1 mA		175		℃
		Reset, temperature decreasing			145		
R_{DISCH}	Output discharge resistance	V_{EN} ≤ 0.2 V, V_{IN} = 5 V（only PJ20030A）			100		Ω
t_{ON}	Turn-on time	From assertion of V_{EN} to V_{OUT} = 90% $V_{OUT(NOM)}$			120		μs

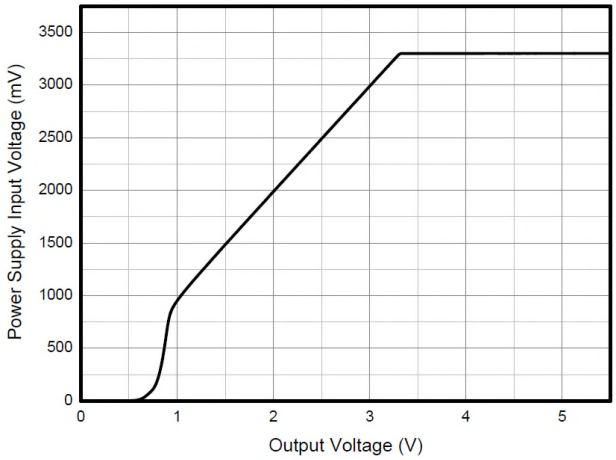
Note:
(1) It is not recommended to use at 125°C without load.
(2) Specifications subject to change without notice.

TYPICAL PERFORMANCE CHARACTERISTIC



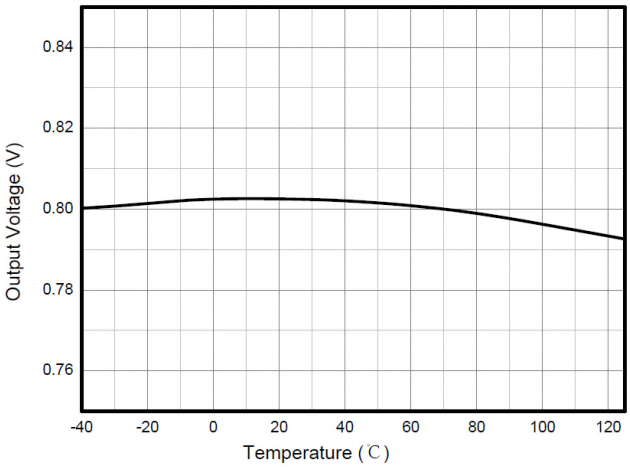
C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{OUT} = 0.8 V

Figure-2. Output voltage vs. Input voltage



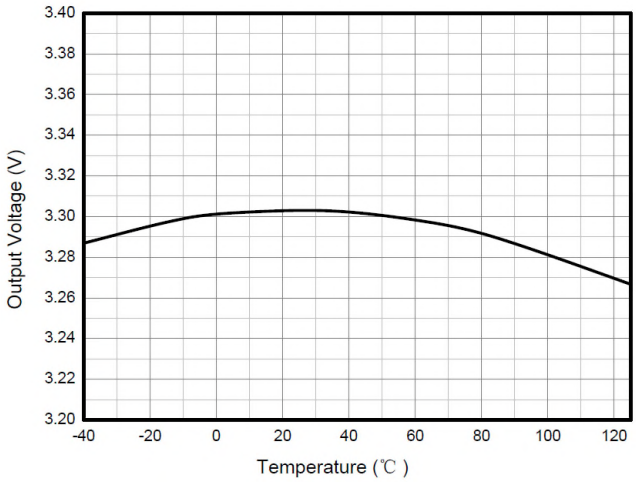
C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{OUT} = 3.3 V

Figure-3. Input voltage vs. Output voltage



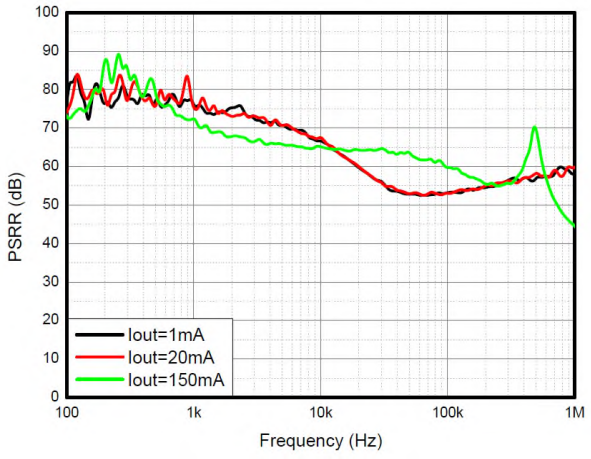
V_{OUT} = 0.8 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA

Figure-4. Output voltage vs. Temperature



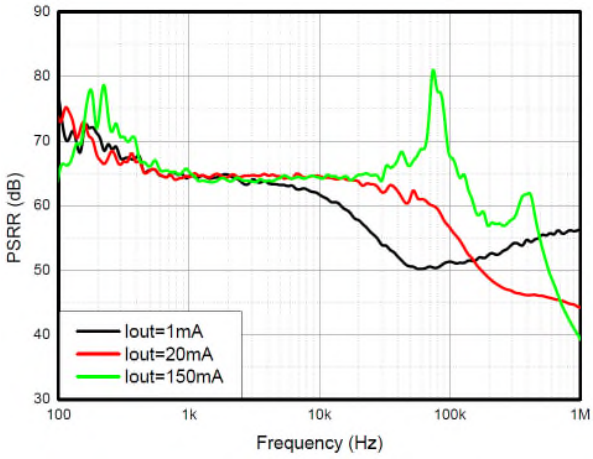
V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA

Figure-5. Output voltage vs. Temperature



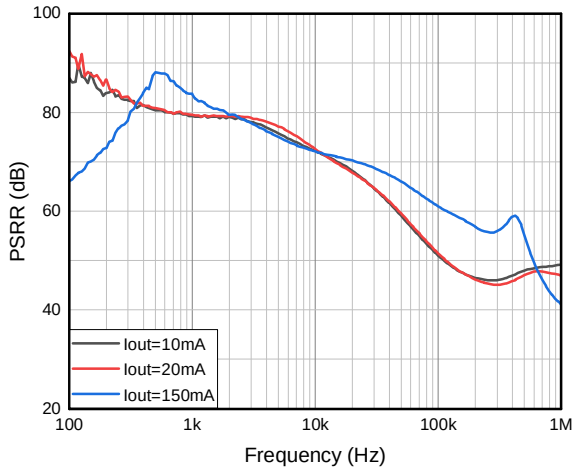
C_{OUT} = 1 µF, V_{IN} = (2.5 V + 200 mVpp), V_{OUT} = 0.8 V

Figure-6. PSRR vs. Frequency



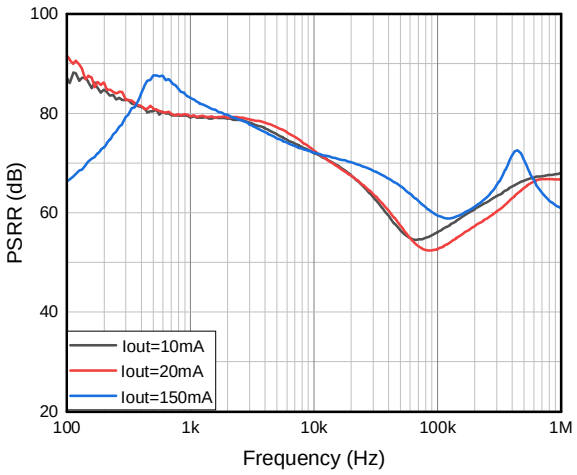
C_{OUT} = 1 µF, V_{IN} = (4.3 V + 200 mVpp), V_{OUT} = 3.3 V

Figure-7. PSRR vs. Frequency



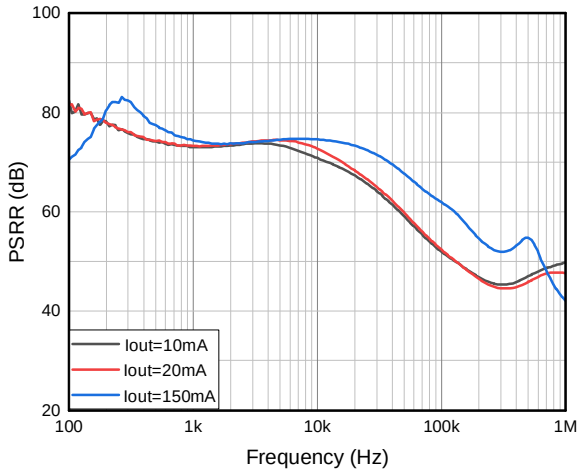
C_{OUT} = 1 µF, V_{IN} = (3 V + 500 mV_{PP}), V_{OUT} = 1.1 V

Figure-8. PSRR vs. Frequency



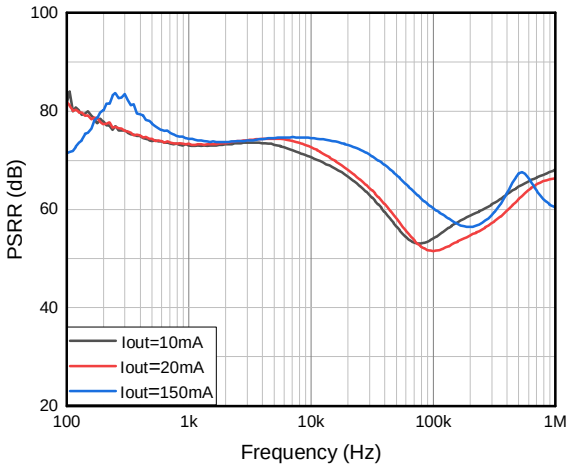
C_{OUT}=10 µF, V_{IN} = (3 V + 500 mV_{PP}), V_{OUT} = 1.1 V

Figure-9. PSRR vs. Frequency



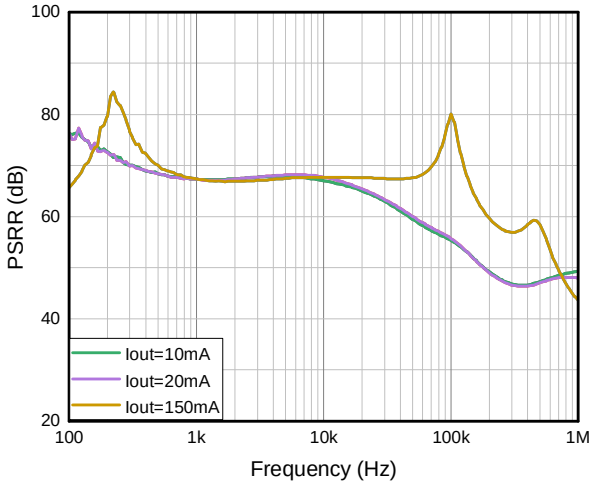
C_{OUT} = 1 µF, V_{IN} = (2.8 V + 500 mV_{PP}), V_{OUT} = 1.8 V

Figure-10. PSRR vs. Frequency



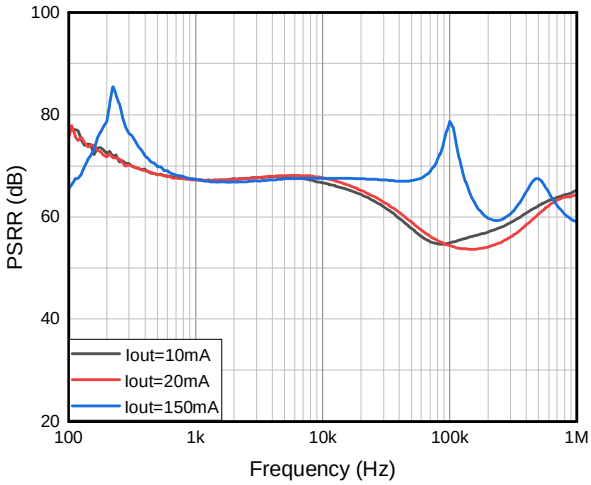
C_{OUT} =10 µF, V_{IN} = (2.8 V + 500 mV_{PP}), V_{OUT} = 1.8 V

Figure-11. PSRR vs. Frequency



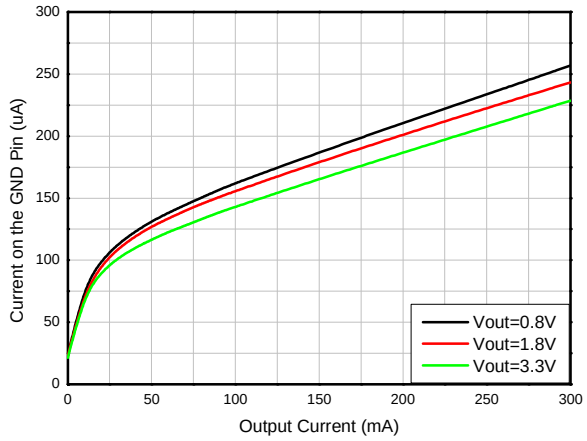
C_{OUT} = 1 µF, V_{IN} = (3.8 V + 500 mV_{PP}), V_{OUT} = 2.8 V

Figure-12. PSRR vs. Frequency



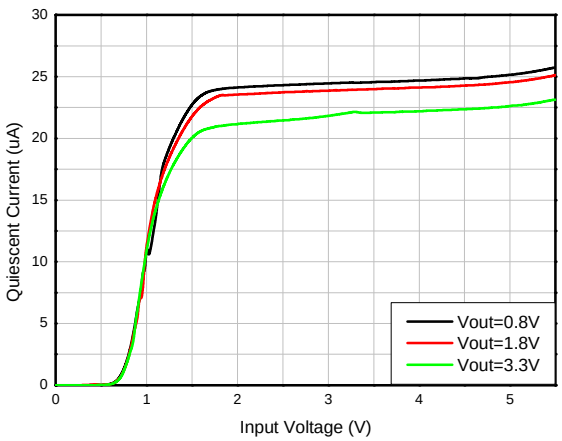
C_{OUT} = 10 µF, V_{IN} = (3.8 V + 500 mV_{PP}), V_{OUT} = 2.8 V

Figure-13. PSRR vs. Frequency



C_{OUT} = 1 µF, V_{IN} = (V_{OUT} + 1 V) or 2.5 V whichever is higher

Figure-14. Current on the GND pin vs. Output current



C_{OUT} = 1 µF, I_{OUT} = 0 mA

Figure-15. Quiescent current vs. Input voltage

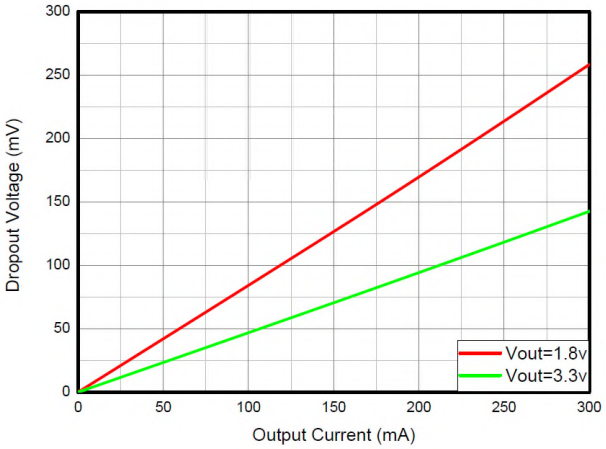
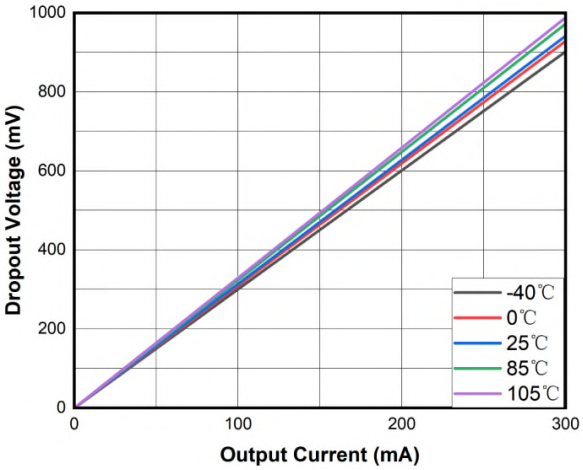
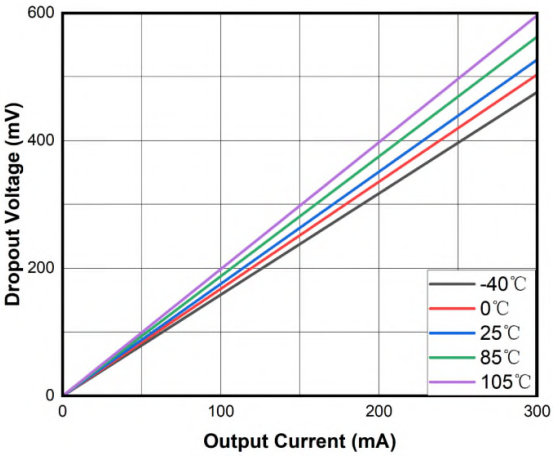


Figure-16. Dropout voltage vs. Output current



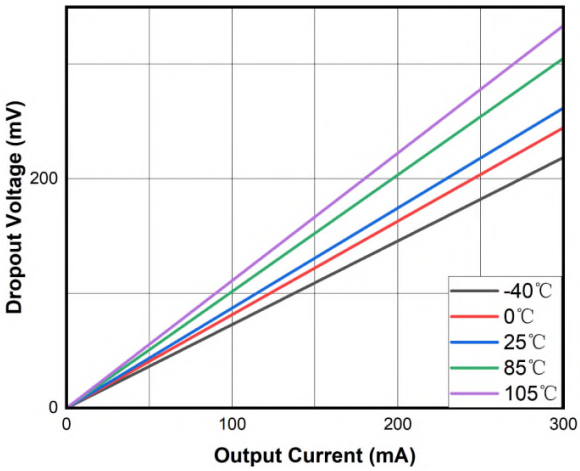
V_{OUT} = 0.8 V, I_L = 300 mA, V_{EN} = 1 V

Figure-17. Dropout voltage vs. Output current



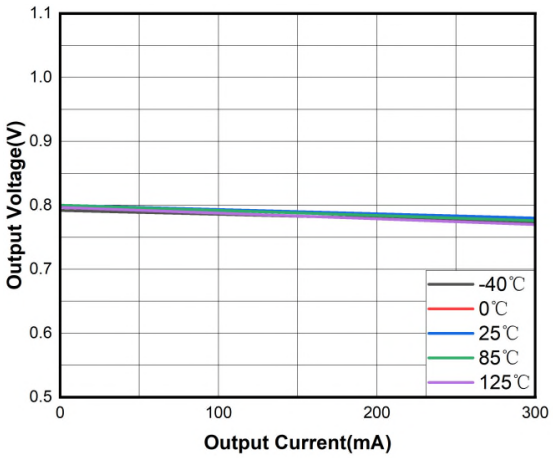
V_{OUT} = 1.2 V, I_L = 300 mA, V_{EN} = 1 V

Figure-18. Dropout voltage vs. Output current



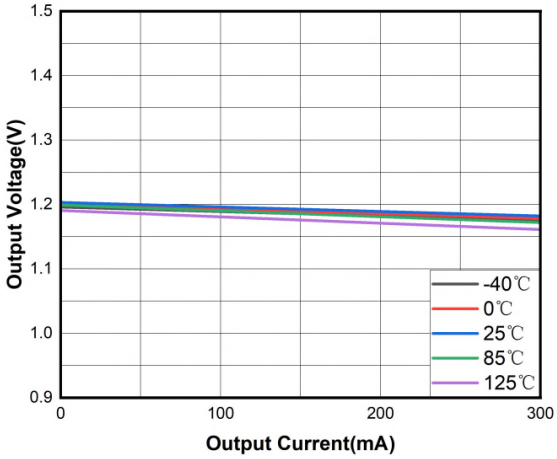
V_{OUT} = 1.8 V, I_L = 300 mA, V_{EN} = 1 V

Figure-19. Dropout voltage vs. Output current



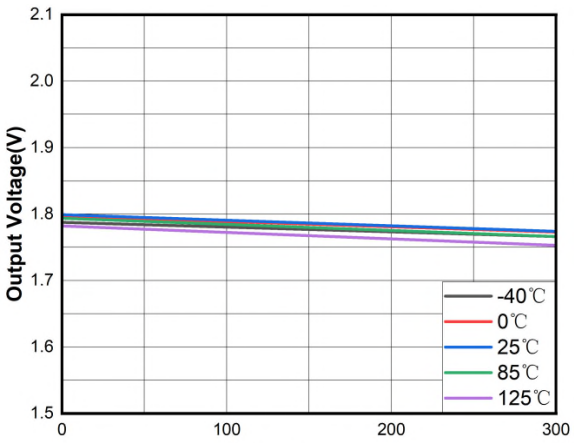
V_{IN} = 2.5 V, V_{OUT} = 0.8 V, V_{EN} = 1 V

Figure-20. Load regulation vs. Output current



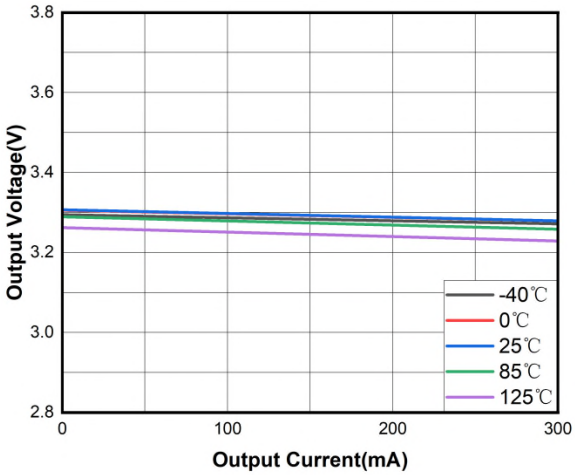
V_{IN} = 2.5 V, V_{OUT} = 1.2 V, V_{EN} = 1 V

Figure-21. Load regulation vs. Output current



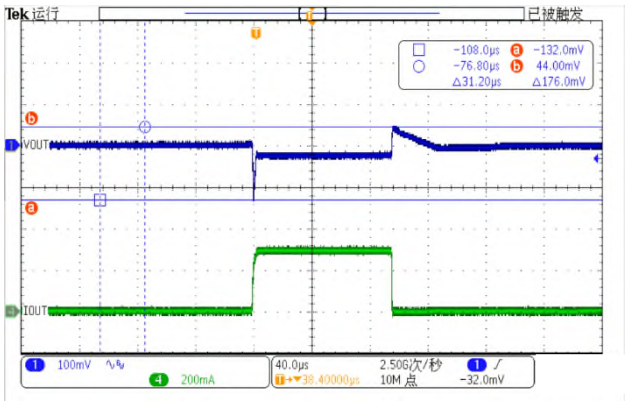
V_{IN} = 2.8 V, V_{OUT} = 1.8 V, V_{EN} = 1 V

Figure-22. Load regulation vs. Output current



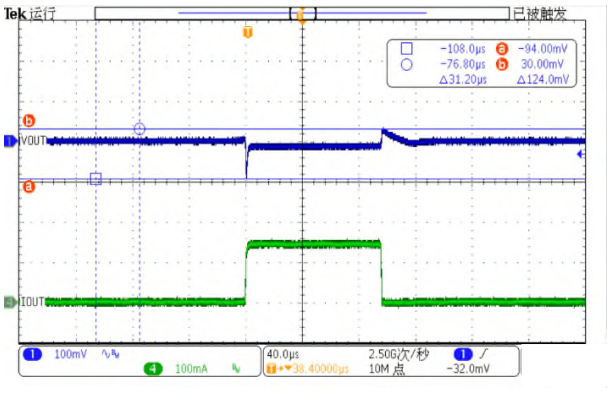
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, V_{EN} = 1 V

Figure-23. Load regulation vs. Output current



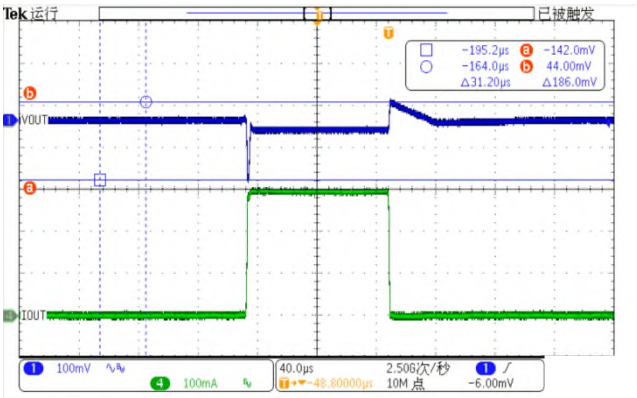
V_{IN} = 2.5 V, V_{OUT} = 0.8 V, C_{IN} = C_{OUT} = 1 µF

Figure-24. Load transient response at load step from 1 mA to 300 mA, V_{OUT} = 0.8 V



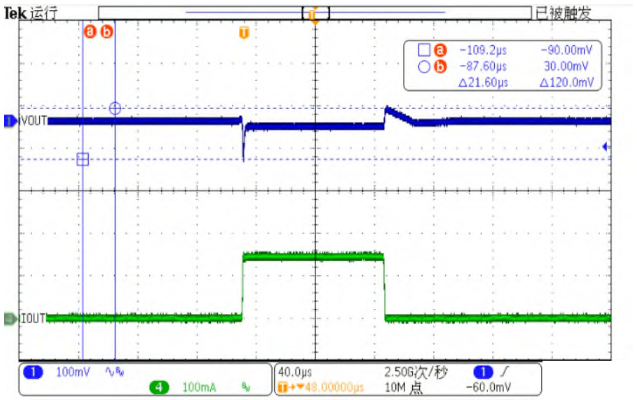
V_{IN} = 2.5 V, V_{OUT} = 0.8 V, C_{IN} = C_{OUT} = 1 µF

Figure-25. Load transient response at load step from 1 mA to 150 mA, V_{OUT} = 0.8 V



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 µF

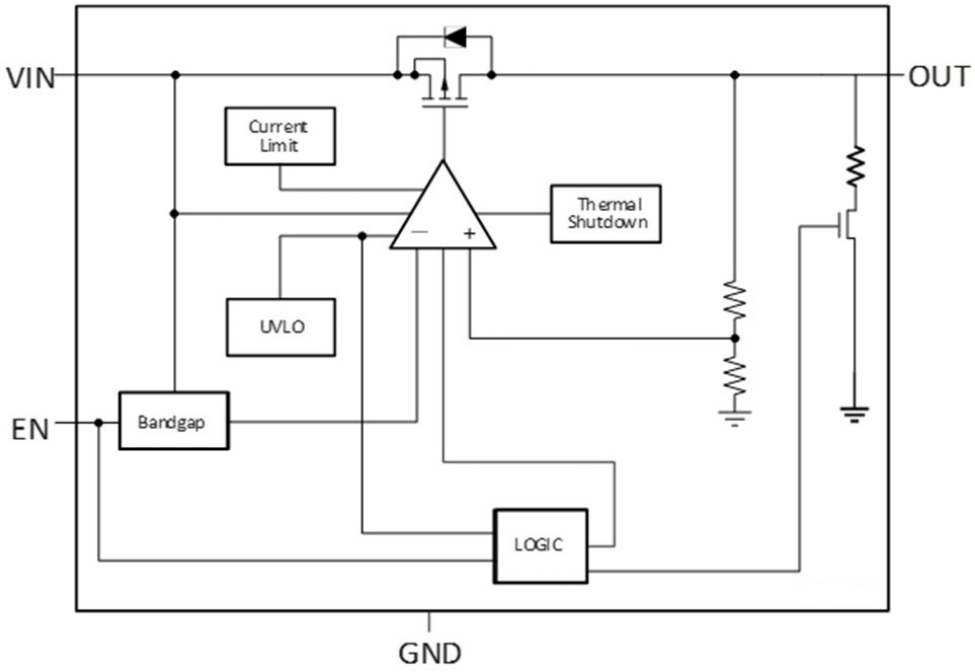
Figure-26. Load transient response at load step from 1 mA to 300 mA, V_{OUT} = 3.3 V



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 µF

Figure-27. Load transient response at load step from 1 mA to 150 mA, V_{OUT} = 3.3 V

FUNCTIONAL BLOCK DIAGRAM



Overview

The PJ20030 series of LDO linear regulators is low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provide overall ±1% accuracy. Low output noise, very high PSRR, and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, and current limit.

Internal current limit

The PJ20030 internal current limit helps to protect the regulator during fault conditions. During the current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated and $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until the thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between the current limit and thermal shutdown.

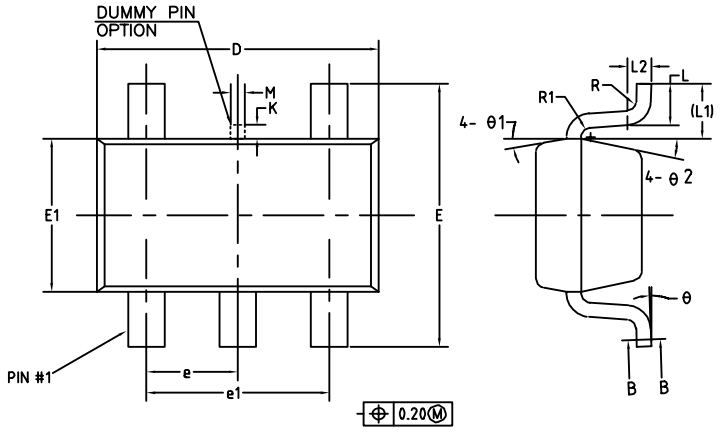
Shut down

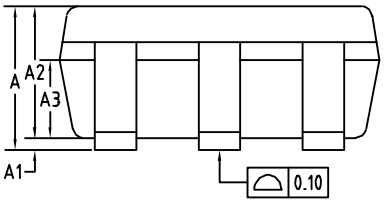
The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 1V. The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

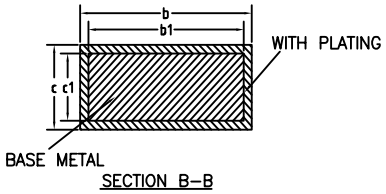
Dropout voltage

The PJ20030 uses a PMOS pass transistor to achieve low dropout. When (VIN – VOUT) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

PACKAGE DIMENSION – SOT23-5

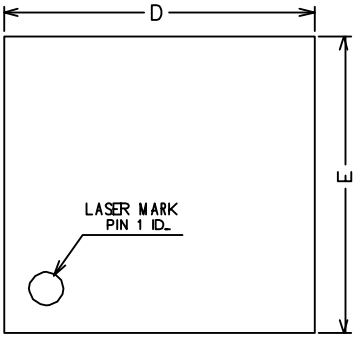




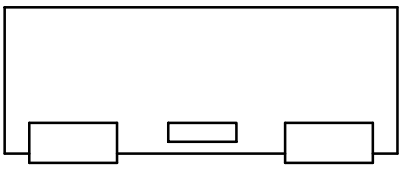


Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Typ**	**Max**
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e 1	1.80	1.90	2.00
K	0	-	0.25
L	0.30	0.40	0.60
L1		0.59 REF	
L2		0.25 BSC	
M	0.10	0.15	0.25
R	0.05	-	0.20
R1	0.05	-	0.20
Θ	0°	-	8°
Θ1	8°	10°	12°
Θ2	10°	12°	14°

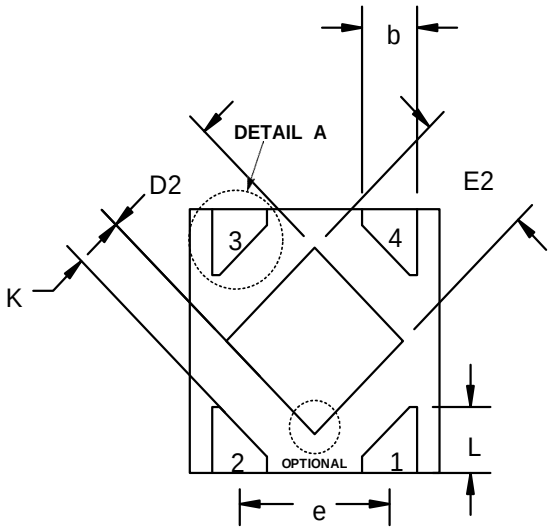
PACKAGE DIMENSION – DFN1x1-4



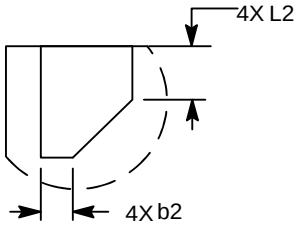
TOP VIEW



SIDE VIEW

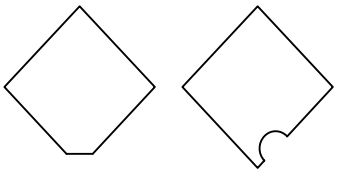


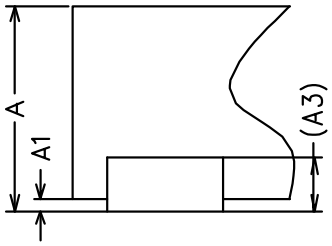
BOTTOM VIEW

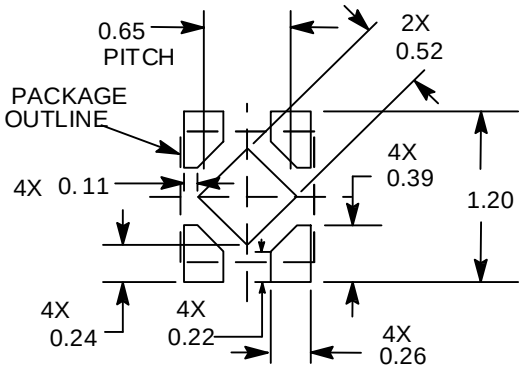


DETAIL A

Two options:





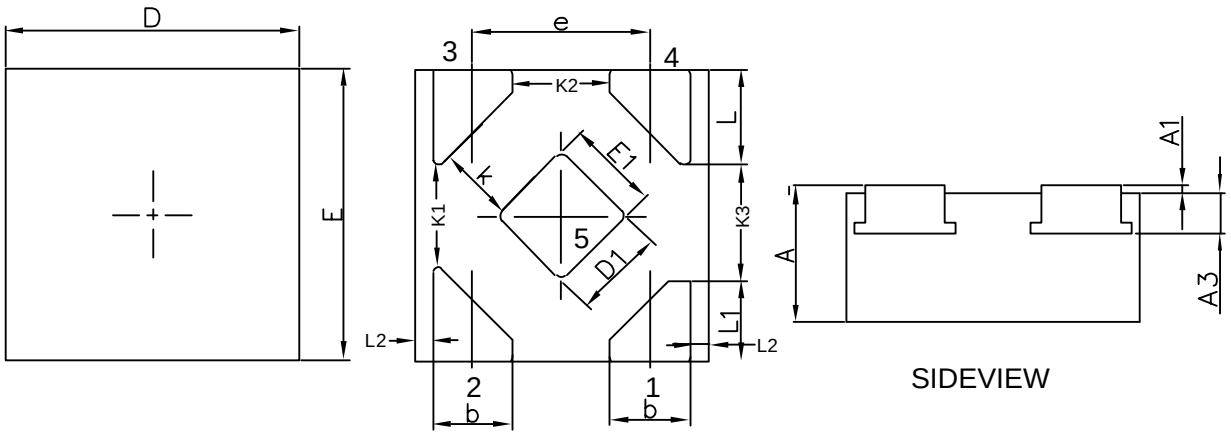


RECOMMENDED LAND PATTERN (Unit: mm)

PACKAGE DIMENSION – DFN1x1-4

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3		0.10 REF	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	0.60	0.65	0.70
K	0.15	-	-
L2	0.07	0.12	0.17
b2	0.02	-	0.12

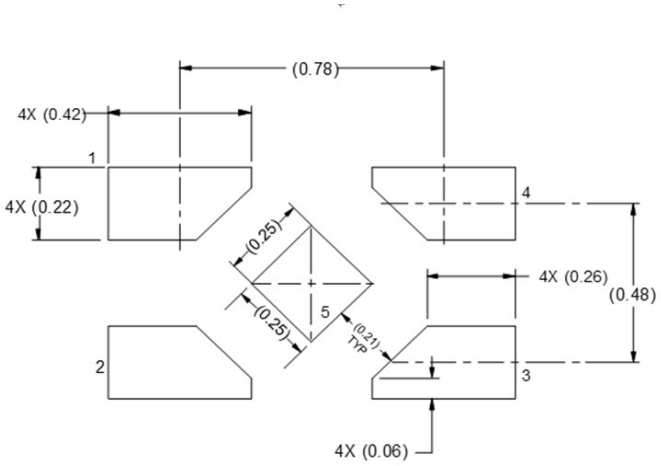
PACKAGE DIMENSION – DFN0.8x0.8-4



TOPVIEW

BOTTOMVIEW

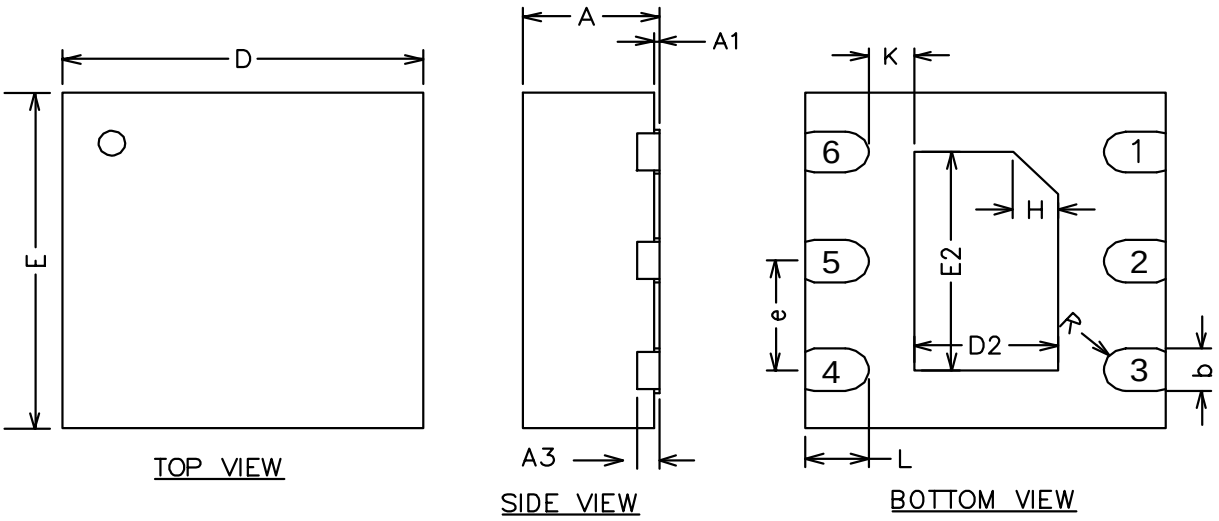
SIDEVIEW

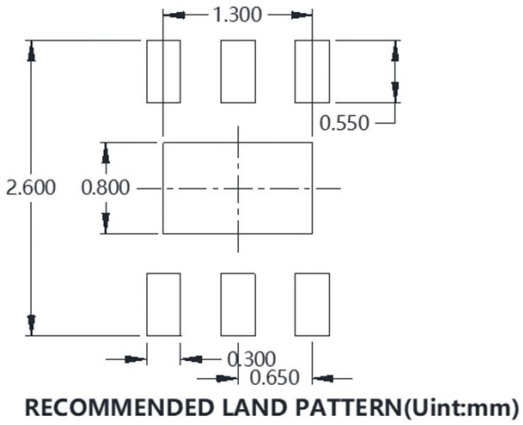


RECOMMENDED LAND PATTERN (Unit: mm)

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.320	0.375	0.400
A1	0.000	0.020	0.050
A3		0.110 REF	
D	0.750	0.800	0.850
E	0.750	0.800	0.850
D1	0.200	0.250	0.300
E1	0.200	0.250	0.300
K		0.210 TYP	
K1		0.270 TYP	
K2		0.260 TYP	
K3		0.315 TYP	
b	0.170	0.220	0.270
e		0.480 TYP	
L	0.210	0.265	0.320
L1	0.170	0.220	0.270
L2		0.050 TYP	

PACKAGE DIMENSION – DFN2x2-6





RECOMMENDED LAND PATTERN(Uint:mm)

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.70	0.80	0.90
E2	1.20	1.30	1.40
e	0.55	0.65	0.75
H		0.25 REF	
K	0.20	-	-
L	0.30	0.35	0.40
R	0.11	-	-

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