



PJS6421-AU

20V P-Channel Enhancement Mode MOSFET

Voltage

-20 V

Current

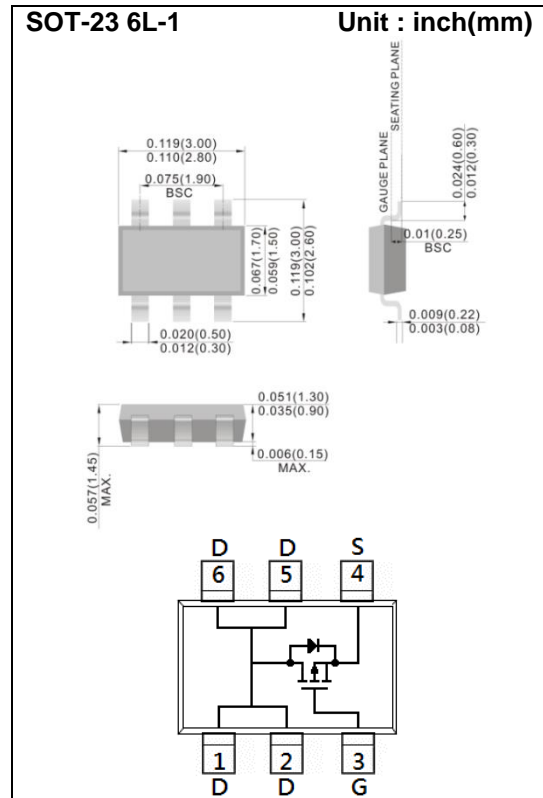
-7.4 A

Features

- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-5A < 26m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-2.5V$, $I_D@-4A < 32m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-1.8V$, $I_D@-3A < 40m\Omega$
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : SOT-23 6L-1 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0005 ounces, 0.014 grams



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current ^(Note 4)	I_D	-7.4	A
Pulsed Drain Current ^(Note 1)	I_{DM}	-29.6	
Power Dissipation	$T_a=25^\circ C$	2	W
	Derate above 25°C	16	mW/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	°C
Typical Thermal Resistance	$R_{\theta JA}$	62.5	°C/W
- Junction to Ambient ^(Note 3,4)			



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.3	-0.55	-1	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-5A	-	21	26	mΩ
		V _{GS} =-2.5V, I _D =-4A	-	26	32	
		V _{GS} =-1.8V, I _D =-3A	-	32	40	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-5A, V _{GS} =-4.5V (Note 1,2)	-	16.5	-	nC
Gate-Source Charge	Q _{gs}		-	2.6	-	
Gate-Drain Charge	Q _{gd}		-	3.1	-	
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ	-	1620	-	pF
Output Capacitance	C _{oss}		-	220	-	
Reverse Transfer Capacitance	C _{rss}		-	160	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =-10V, I _D =-1A, V _{GS} =-4.5V, R _G =25Ω (Note 1,2)	-	22	-	ns
Turn-On Rise Time	t _r		-	25	-	
Turn-Off Delay Time	t _{d(off)}		-	138	-	
Turn-Off Fall Time	t _f		-	53	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-2	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V	-	-0.7	-1	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

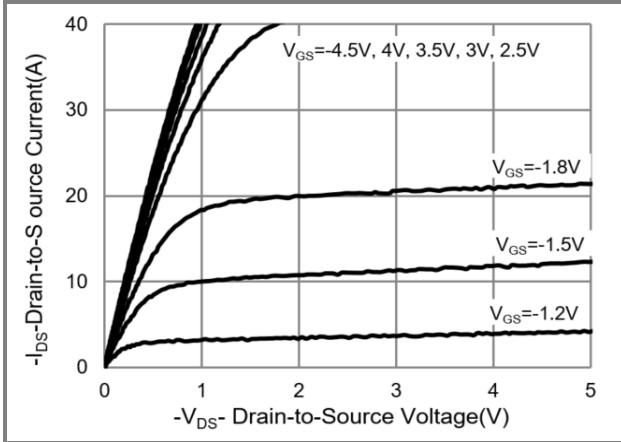


Fig.1 On-Region Characteristics

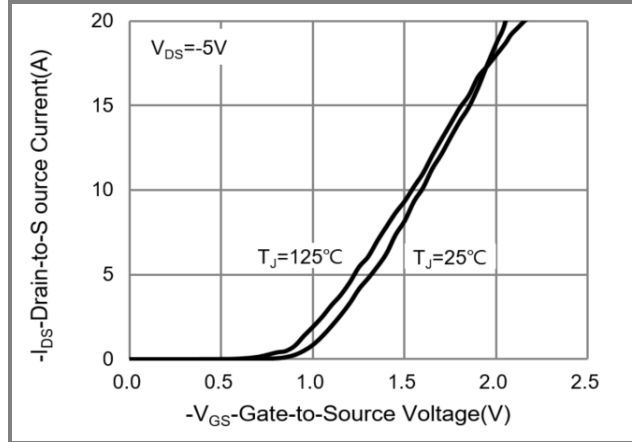


Fig.2 Transfer Characteristics

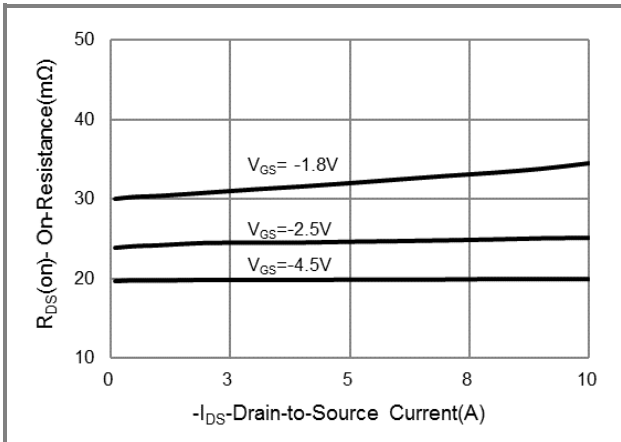


Fig.3 On-Resistance vs. Drain Current

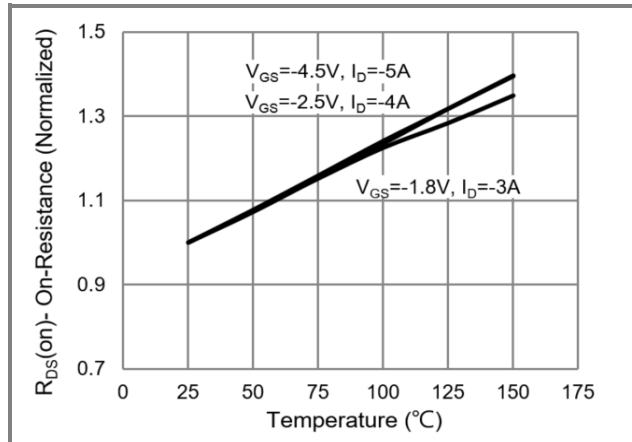


Fig.4 On-Resistance vs. Junction temperature

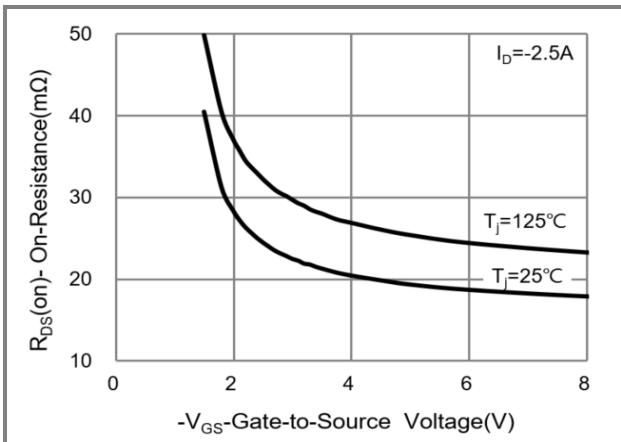


Fig.5 On-Resistance Variation with V_{GS}

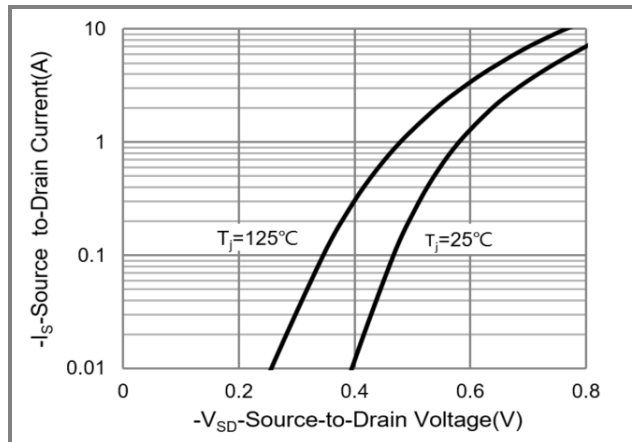


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

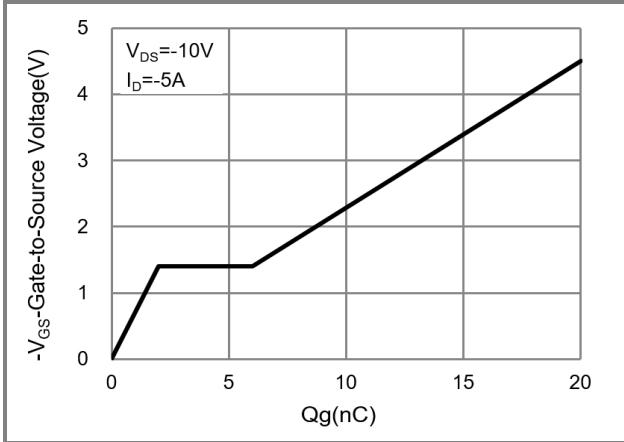


Fig.7 Gate-Charge Characteristics

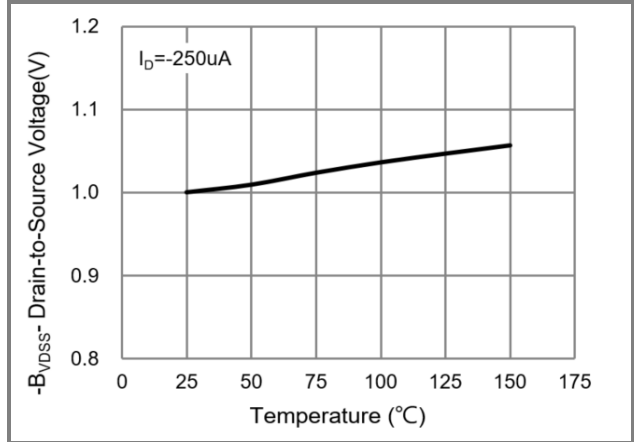


Fig.8 Breakdown Voltage Variation vs. Temperature

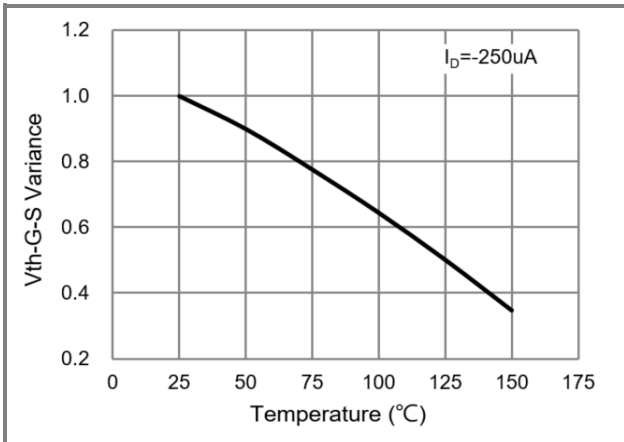


Fig.9 Threshold Voltage Variation with Temperature

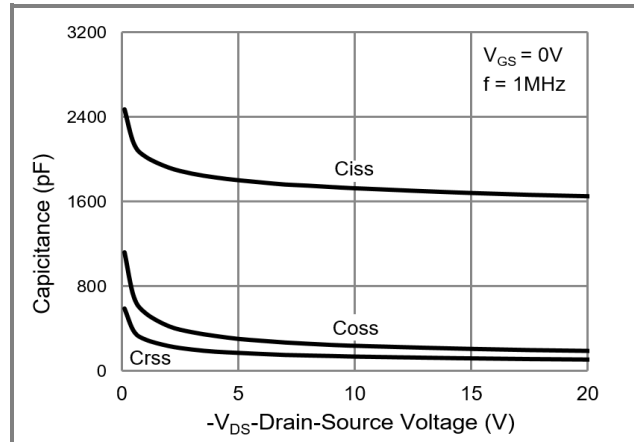


Fig.10 Capacitance vs. Drain-Source Voltage

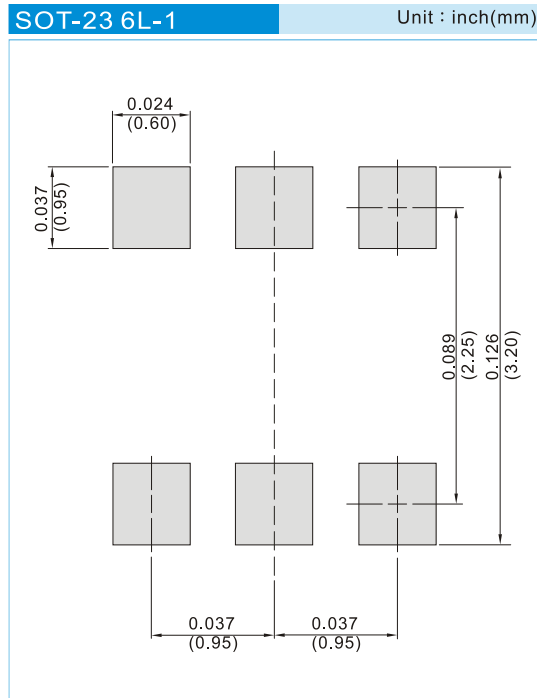


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Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJS6421-AU_S1_000A1	SOT-23 6L-1	3K pcs / 7" reel	S21	Halogen free RoHS compliant

Mounting Pad Layout





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