30V N-Channel Enhancement Mode MOSFET

Voltage

ΡΛΝ

Current 45 A

Features

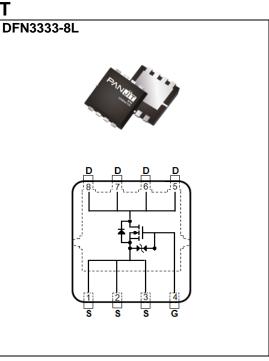
• $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@10A < 7.8m\Omega$

30 V

- Rds(on), Vgs@4.5V, Id@6A<13m Ω
- Excellent FOM
- Logic Level Drive
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current ^(Note 3)	T _C =25°C		45	
	Tc=100°C	I _D	28	А
Pulsed Drain Current ^(Note 1)	T _C =25°C	I _{DM}	180	
Power Dissipation	T _C =25°C		25	
	Tc=100°C	PD	10	W
Continuous Drain Current ^(Note 4)	T _A =25°C		13	
	T _A =70°C	I _D	10.3	— A
Power Dissipation	T _A =25°C	Pp	2.1	W
	T _A =70°C	PD	1.3	vv
Single Pulse Avalanche Energy ^(Note 5)		Eas	18	mJ
Operating Junction and Storage Temperature Range		TJ,TSTG	-55~150	°C
Thermal Resistance ^(Note 4)	Junction to Case	R _{θJC}	5	°C/W
	Junction to Ambient	R _{θJA}	60	C/W



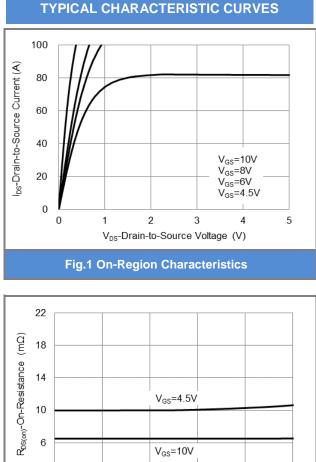
Electrical Characteristics (TA=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS	
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	30	-	-	V	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.3	1.7	2.5		
Drain-Source On-State Resistance	R _{DS(on)}	V_{GS} =10V, I_{D} =10A	-	6.5	7.8	mΩ	
		V _{GS} =4.5V, I _D =6A	-	10	13		
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} =30V, V_{GS} =0V	-	-	±1	uA	
Gate-Source Leakage Current	I _{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±10	uA	
Dynamic ^(Note 6)	-		•	•	•		
Total Gate Charge	Qg		-	12.4	-		
Gate-Source Charge	Qgs	V _{DS} =24V, I _D =10A, V _{GS} =10V ^(Note 2,3)	-	2	-	nC	
Gate-Drain Charge	Q_{gd}	VGS=10V(((1010-2,0))	-	3.4	-		
Input Capacitance	Ciss		-	600	-	pF	
Output Capacitance	Coss	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	254	-		
Reverse Transfer Capacitance	Crss		-	71	-		
Gate resistance	Rg	f=1MHz	-	1.1	-	Ω	
Turn-On Delay Time	td _(on)		-	9	-		
Turn-On Rise Time	tr	V _{DS} =24V, I _D =10A,	-	10	-		
Turn-Off Delay Time	td _(off)	V _{GS} =10V, R _G =3Ω	-	20	-	ns	
Turn-Off Fall Time	tf	(14016 2,5)	-	16	-		
Drain-Source Diode	-		-	-	-		
Diode Forward Current	I _S	T 0500	-	-	45		
Pulsed Diode Forward Current	I _{SM}	Tc=25°C	-	-	180	A	
Diode Forward Voltage	V _{SD}	Is=20A, V _{GS} =0V	-	0.8	1.1	V	
Reverse Recovery Time	Trr	V _{GS} =0V, I _S =20A	-	25	-	ns	
Reverse Recovery Charge	Qrr	dls/dt=100A/us ^(Note 2,3)	-	11	-	nC	

NOTES :

- 1. Pulse width \leq 100us, Duty cycle \leq 2%.
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Chip capability with an $R_{\theta JC}=5^{\circ}C/W$.
- 4. $R_{\theta,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 5. The test condition is L=0.5mH, I_{AS} =9A, V_{DD} =30V, V_{GS} =10V, Starting T_J =25°C. the chip is about to carry I_{AS} ≈17A.
- 6. Guaranteed by design, not subject to production testing.





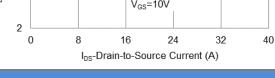
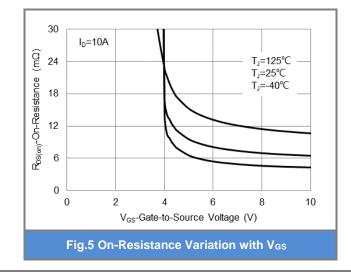


Fig.3 On-Resistance vs. Drain Current



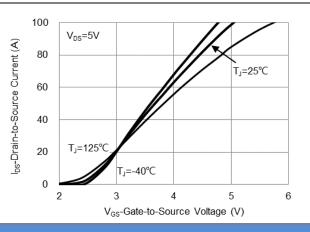


Fig.2 Transfer Characteristics

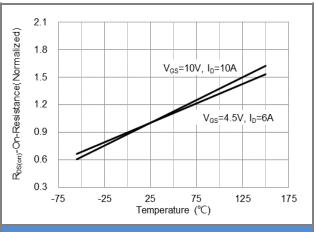
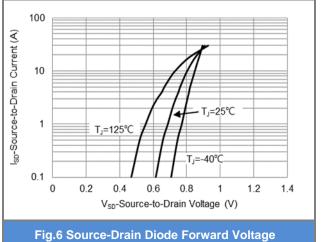
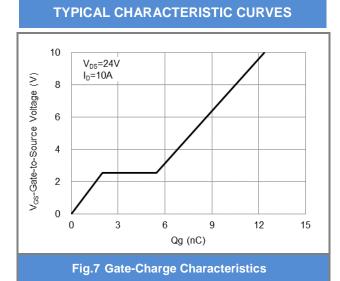
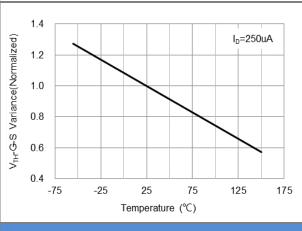


Fig.4 On-Resistance vs. Junction temperature

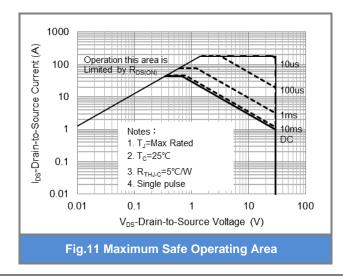


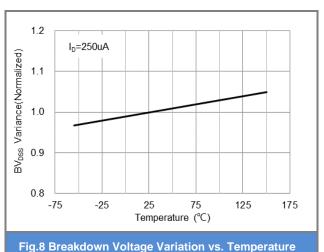












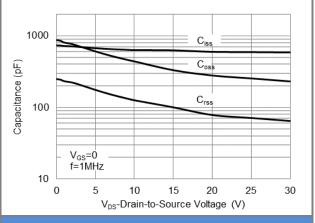
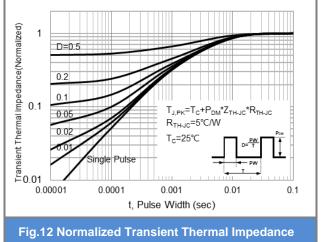


Fig.10 Capacitance vs. Drain-Source Voltage

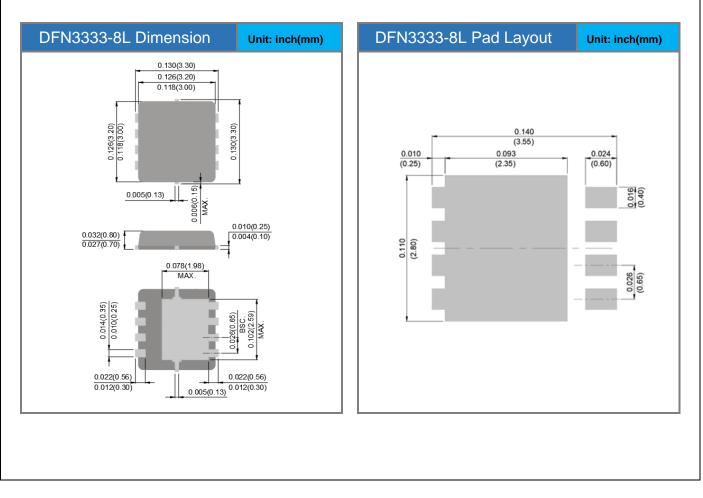




Product and Packing Information

Part No.	Package Type	Packing Type	Marking	
PJQ4530P	DFN3333-8L	5K pcs / 13" reel	4530	

Packaging Information & Mounting Pad Layout





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