

### **30V N-Channel Enhancement Mode MOSFET**

Voltage

Current 55 A

#### Features

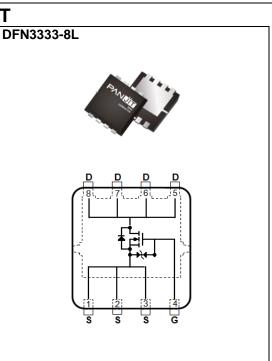
•  $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@12A < 6.5m\Omega$ 

30 V

- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@9A < 10.5m\Omega$
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

#### **Mechanical Data**

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams



### Maximum Ratings and Thermal Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETE	R	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V <sub>DS</sub>	30	V	
Gate-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Droin Curront(Note 3)	T <sub>C</sub> =25°C		55		
Continuous Drain Current <sup>(Note 3)</sup>	Tc=100°C	I <sub>D</sub>	39	А	
Pulsed Drain Current <sup>(Note 1)</sup>	T <sub>C</sub> =25°C	I <sub>DM</sub>	220		
Power Dissipation	T <sub>C</sub> =25°C	D-	32	14/	
	Tc=100°C	PD	16	W	
Continuous Drain Current <sup>(Note 4)</sup>	T <sub>A</sub> =25°C		15.5	٥	
	T <sub>A</sub> =70°C	I <sub>D</sub>	13	— A	
Power Dissipation $\begin{array}{c} T_{A}=25^{\circ}C \\ T_{A}=70^{\circ}C \end{array} \qquad Pr$	Da	2.5	W		
	T <sub>A</sub> =70°C	PD	1.8	VV	
Single Pulse Avalanche Energy <sup>(Note 5)</sup>		Eas	44	mJ	
Operating Junction and Storage Temperature Range		TJ,TSTG	-55~175	°C	
Thormal Pacietanco(Note 4)	Junction to Case	R <sub>θJC</sub>	4.7	0000	
Thermal Resistance <sup>(Note 4)</sup>	Junction to Ambient	R <sub>θJA</sub>	60	°C/W	



### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

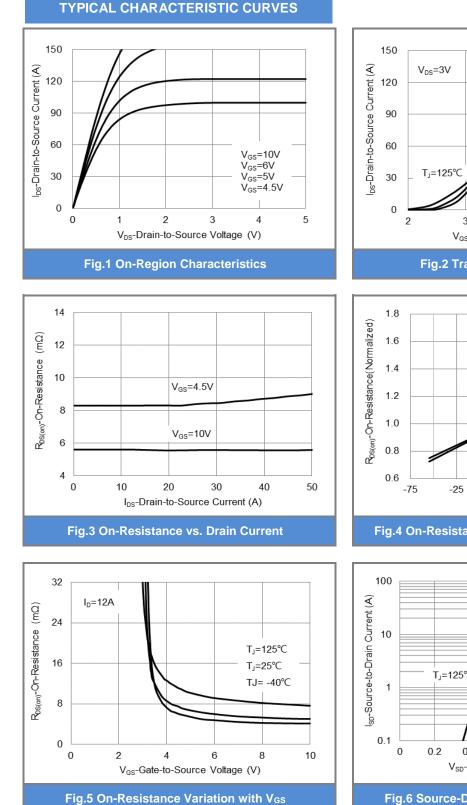
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS	
Static							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.2	1.76	2.5		
	_	V <sub>GS</sub> =10V, I <sub>D</sub> =12A -		5.6	6.5		
Drain-Source On-State Resistance	ain-Source On-State Resistance R <sub>DS(on)</sub> V <sub>GS</sub> =4.5V, I <sub>D</sub> =9A		-	8.3	10.5	mΩ	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ =30V, $V_{GS}$ =0V	-	-	1	uA	
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	uA	
Dynamic <sup>(Note 6)</sup>							
Total Gate Charge	Qg		-	10.7	-	nC	
Gate-Source Charge	Qgs	V <sub>DS</sub> =15V, I <sub>D</sub> =12A, V <sub>GS</sub> =10V <sup>(Note 2,3)</sup>	-	2	-		
Gate-Drain Charge	$Q_{gd}$	VGS=10V(((000 2,0))	-	2.2	-		
Input Capacitance	Ciss		-	785	-	pF	
Output Capacitance	Coss	$V_{DS}$ =15V, $V_{GS}$ =0V,	-	375	-		
Reverse Transfer Capacitance	Crss	f=1MHz	-	25	-		
Gate resistance	Rg	f=1MHz	-	2	-	Ω	
Turn-On Delay Time	td <sub>(on)</sub>		-	9	-		
Turn-On Rise Time	tr	V <sub>DS</sub> =15V, I <sub>D</sub> =1A,	-	2	-		
Turn-Off Delay Time	td <sub>(off)</sub>	V <sub>GS</sub> =10V, R <sub>G</sub> =1Ω (Note 2,3)	-	20	-	ns	
Turn-Off Fall Time	tf	(11012 2,3)	-	7	-		
Drain-Source Diode	·						
Diode Forward Current	I <sub>S</sub>	T 0500	-	-	55	A	
Pulsed Diode Forward Current	I <sub>SM</sub>	Tc=25°C	-	-	220		
Diode Forward Voltage	V <sub>SD</sub>	Is=10A, V <sub>GS</sub> =0V	-	0.83	1.1	V	
Reverse Recovery Time	Trr	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	14	-	ns	
Reverse Recovery Charge	Qrr	dls/dt=100A/us <sup>(Note 2,3)</sup>	-	13	-	nC	

NOTES :

- 1. Pulse width100us, Duty cycle<2%.</td>
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Chip capability with an  $R_{\theta JC}$ =4.7°C/W.
- 4.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
- 5. The test condition is L=0.5mH, I\_{AS}=13A, V\_{DD}=30V, V\_{GS}=10V, Starting TJ=25°C.
- 6. Guaranteed by design, not subject to production testing.

SEMI CONDUCTOR

PANJ



 $\begin{array}{c} I_{1}\\ I_{2}\\ I_{3}\\ I_$ 

T\_=25℃

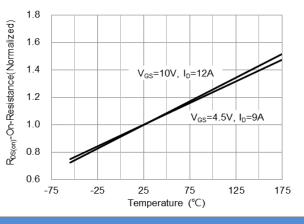
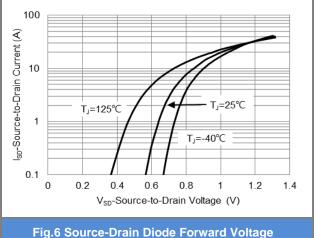


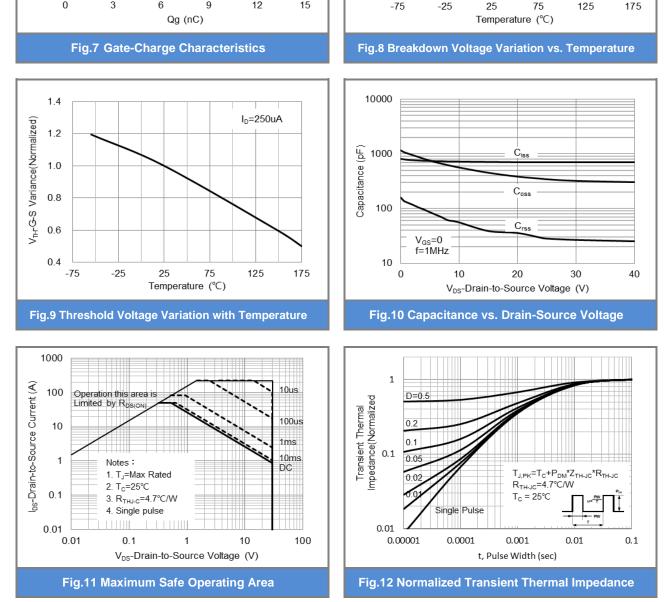
Fig.4 On-Resistance vs. Junction temperature



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1.2

1.1

1.0

0.9

0.8

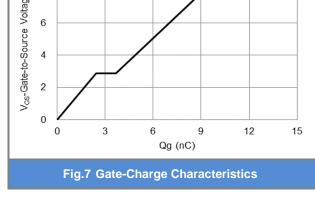
BV<sub>DSS</sub> Variance(Normalized)

I<sub>D</sub>=250uA

#### **TYPICAL CHARACTERISTIC CURVES**

PJQ4528P-AU

10 V<sub>DS</sub>=15V V<sub>os</sub>-Gate-to-Source Voltage (V) I<sub>D</sub>=12A 8 6 4 2 0 0 3 6 9 12 15



PANJ SEM CONDUCTOR

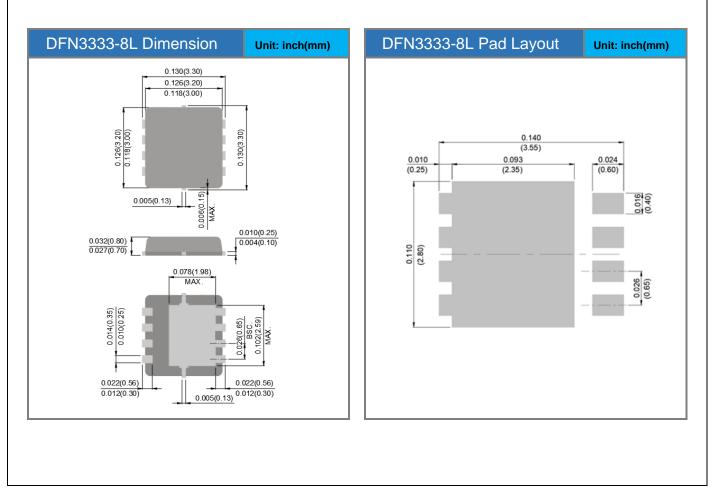




#### **Product and Packing Information**

Part No.	Package Type	Packing Type	Marking	
PJQ4528P-AU	DFN3333-8L	5K pcs / 13" reel	4528	

### Packaging Information & Mounting Pad Layout





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