



60V N-Channel Enhancement Mode MOSFET

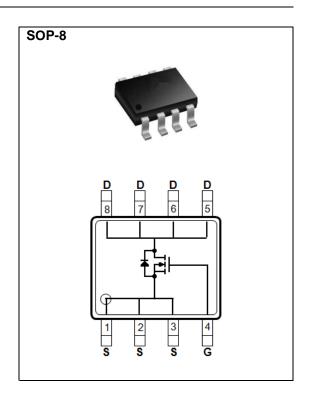
Voltage 60 V Current 10 A

Features

- RDS(ON), VGS@10V, ID@10A<12mΩ
- RDS(ON), VGS@4.5V, ID@5.0A<15mΩ
- Advanced Trench Process Technology
- · High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9434A



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V_{GS}	<u>+</u> 20	V	
Continuous Drain Current	T _A =25°C	I _D	10	А	
	T _A =70°C		8		
Pulsed Drain Current (Note 1)		I _{DM}	40	А	
Power Dissipation	T _A =25°C		2.5	W	
	T _A =70°C	P_{D}	1.6		
Single Pulse Avalanche Energy (Note 5)		E _{AS}	5.0	mJ	
Operating Junction and Storage Temperature Range		T_{J}, T_{STG}	-55~150	°C	
Typical Thermal resistance					
- Junction to Ambient, t≦10s ^(Note 6)		$R_{\theta JA}$	50	°C/W	





Electrical Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS	
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	V_{GS} =0V, I_D =250uA	60	-	-	V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250uA$	1.0	1.7	2.5	V	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V,I _D =10A	-	10.5	12	mΩ	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V,I _D =5A	-	12	15	mΩ	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1.0	uA	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 20V,V _{DS} =0V	-	-	<u>+</u> 100	nA	
Dynamic (Note 7)							
Total Gate Charge	Q_g	V _{DS} =30V, I _D =10A, V _{GS} =10V ^(Note 1,2)	-	39	-	nC	
Gate-Source Charge	Q_gs		-	6.1	-		
Gate-Drain Charge	Q_gd		-	6.7	-		
Input Capacitance	Ciss	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	-	2256	-	pF	
Output Capacitance	Coss		-	145	-		
Reverse Transfer Capacitance	Crss		-	93	-		
Turn-On Delay Time	td _(on)	V_{DD} =15V, I_{D} =10A, V_{GS} =10V, R_{G} =6 Ω (Note 1,2)	-	7.5	-	ns	
Turn-On Rise Time	tr		-	36	-		
Turn-Off Delay Time	td _(off)		-	49	-		
Turn-Off Fall Time	tf		-	12	-		
Drain-Source Diode							
Maximum Continuous Drain-Source	,		-	-	10	А	
Diode Forward Current	I _S						
Diode Forward Voltage	V_{SD}	I _S =1.0A, V _{GS} =0V	-	0.67	1.0	V	

NOTES:

- 1. Pulse width<300us, Duty cycle<2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
- 5. The test condition is L=0.1mH, I_{AS} =10A, V_{DD} =50V, V_{GS} =10V
- 6. Rejah is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 7. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTIC CURVES

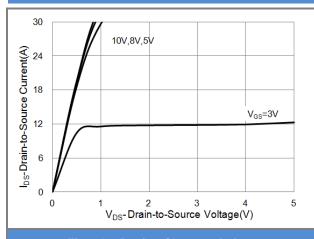


Fig.1 On-Region Characteristics

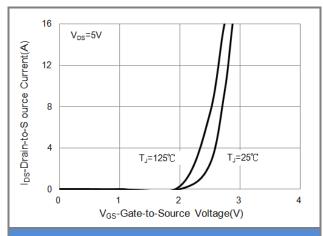


Fig.2 Transfer Characteristics

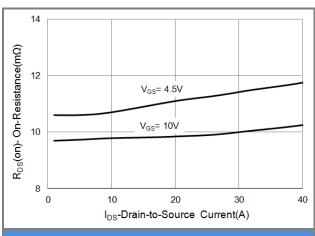


Fig.3 On-Resistance vs. Drain Current

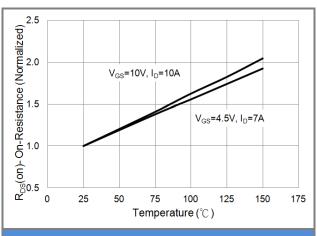


Fig.4 On-Resistance vs. Junction temperature

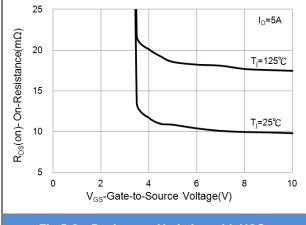


Fig.5 On-Resistance Variation with VGS.

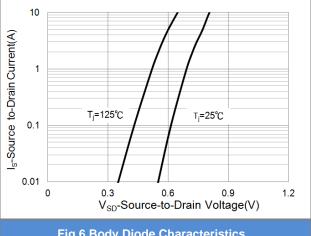


Fig.6 Body Diode Characteristics





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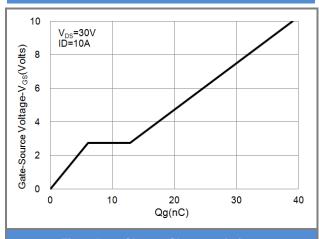


Fig.7 Gate-Charge Characteristics

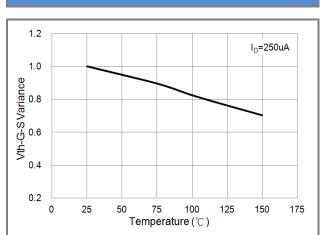
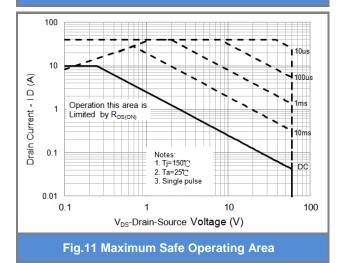


Fig.9 Threshold Voltage Variation with Temperature.



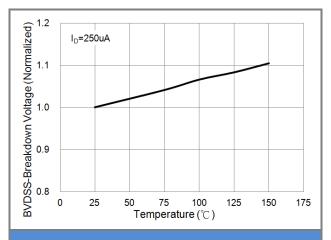


Fig.8 Breakdown Voltage Variation vs. Temperature

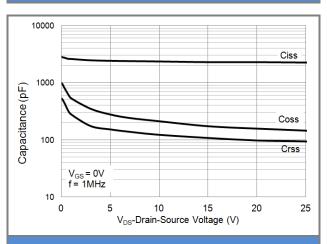


Fig.10 Capacitance vs. Drain-Source Voltage.





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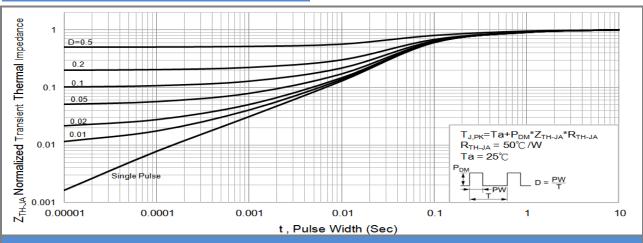


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

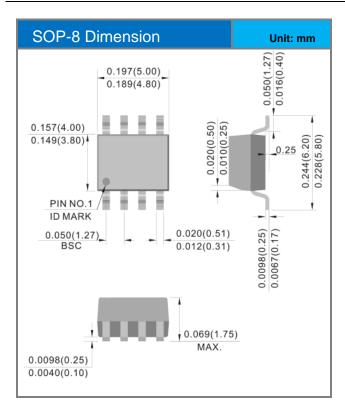


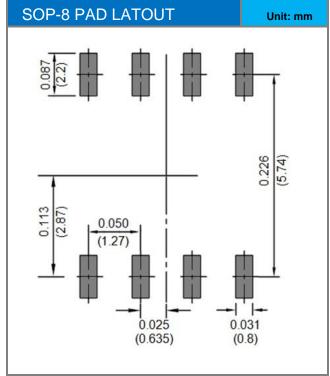


PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9434A_R2_00001	SOP-8	2.5K pcs / 13" reel	L9434A	Halogen free

Packaging Information & Mounting Pad Layout









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