



# PJD50N10AL-AU

## 100V N-Channel Enhancement Mode MOSFET

**Voltage**

**100 V**

**Current**

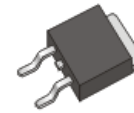
**42 A**

### Features

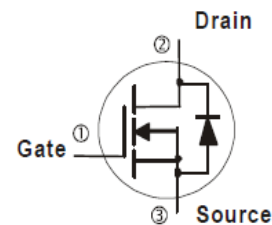
- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A < 25m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@15A < 28.5m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case: TO-252AA Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0104 ounces, 0.297 grams



TO-252AA



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C=25^\circ C$	$I_D$	42	A
	$T_C=100^\circ C$		26	
Pulsed Drain Current (Note 1)	$T_C=25^\circ C$	$I_{DM}$	150	
Power Dissipation	$T_C=25^\circ C$	$P_D$	83	W
	$T_C=100^\circ C$		33	
Continuous Drain Current	$T_A=25^\circ C$	$I_D$	6.3	A
	$T_A=70^\circ C$		5.1	
Power Dissipation	$T_A=25^\circ C$	$P_D$	2.0	W
Power Dissipation	$T_A=70^\circ C$		1.3	
Single Pulse Avalanche Energy (Note 6)		$E_{AS}$	63.4	mJ
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	$^\circ C$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	1.5	$^\circ C/W$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	20	25	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$	-	22	28.5	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>Dynamic</b> (Note 7)						
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$ (Note 1,2)	-	29	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.5	-	
Gate-Drain Charge	$Q_{gd}$		-	6.4	-	
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	1485	-	pF
Output Capacitance	$C_{oss}$		-	135	-	
Reverse Transfer Capacitance	$C_{rss}$		-	67	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=10A,$ $V_{GS}=10V,$ $R_G=3\Omega$ (Note 1,2)	-	7.8	-	ns
Turn-On Rise Time	$t_r$		-	30	-	
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	
Turn-Off Fall Time	$t_f$		-	14	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	42	A
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$	-	0.7	1.2	V

**NOTES :**

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
4. The maximum current rating is package limited.
5.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz. square pad of copper.
6. The test condition is  $L=3\text{mH}, I_{AS}=6.5A, V_{DD}=25V, V_{GS}=10V$
7. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

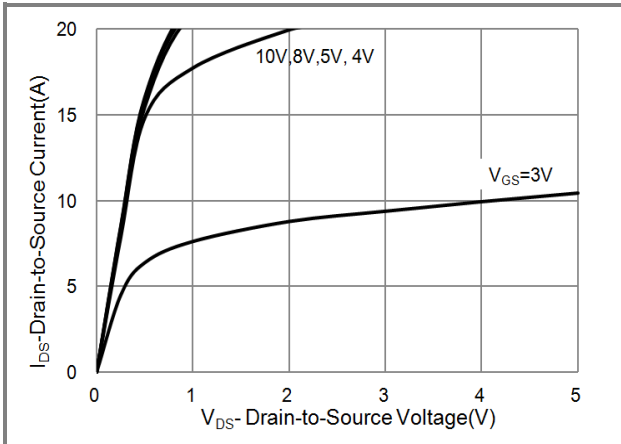


Fig.1 Output Characteristics

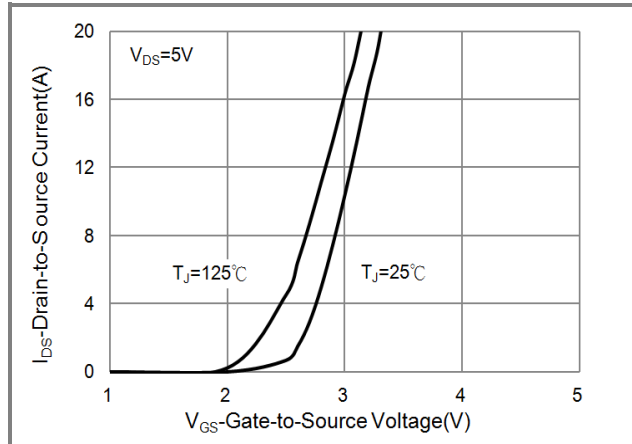


Fig.2 Transfer Characteristics

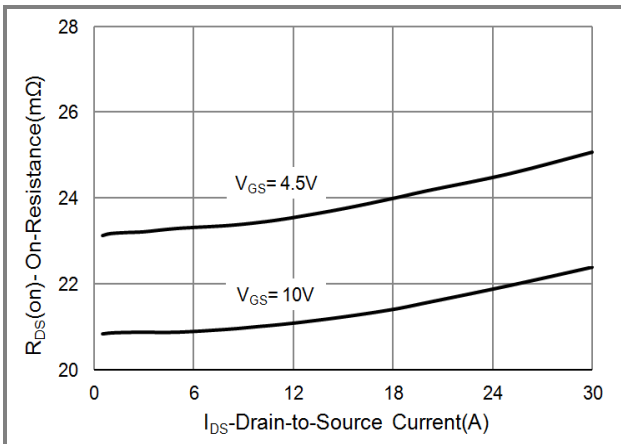


Fig.3 On-Resistance vs. Drain Current

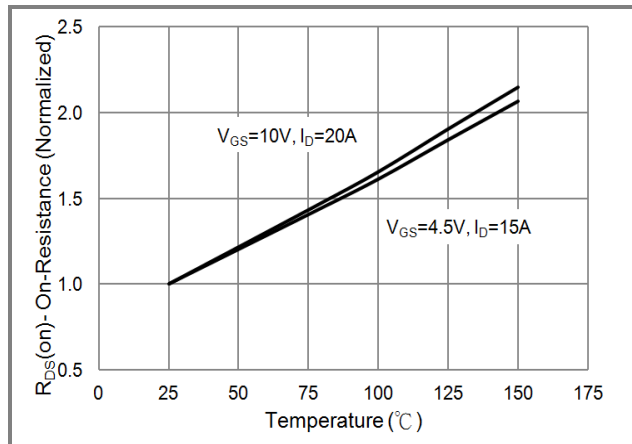


Fig.4 On-Resistance vs. Junction temperature

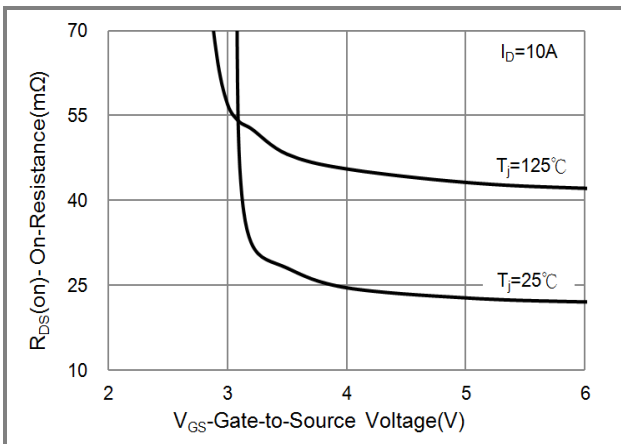


Fig.5 On-Resistance Variation with  $V_{GS}$

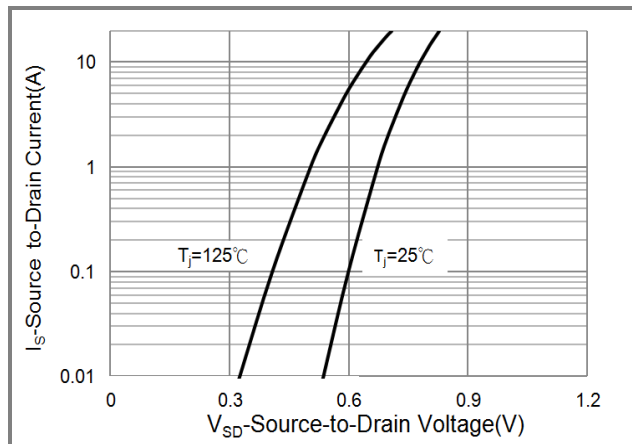


Fig.6 Source-Drain Diode Forward Voltage



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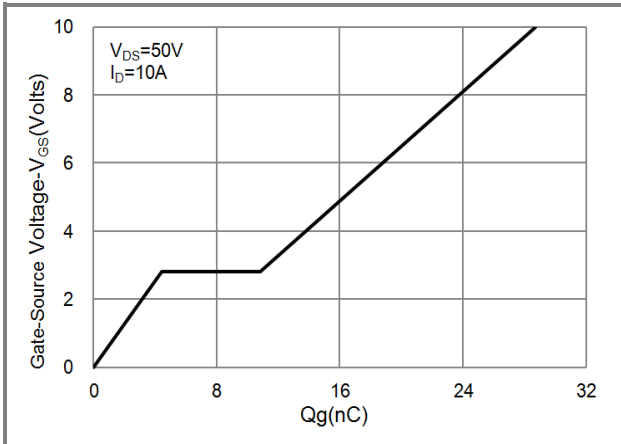


Fig.7 Gate-Charge Characteristics

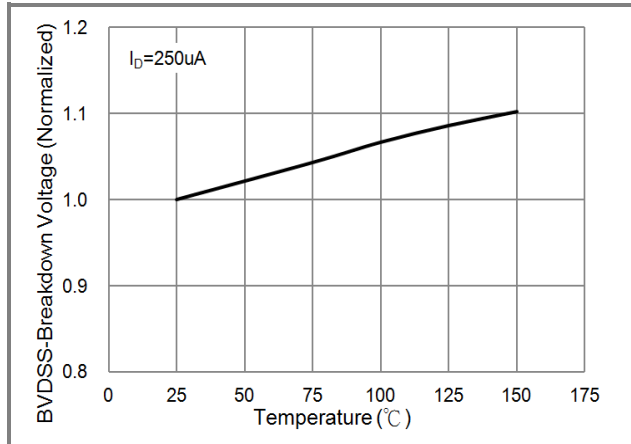


Fig.8 Breakdown Voltage Variation vs. Temperature

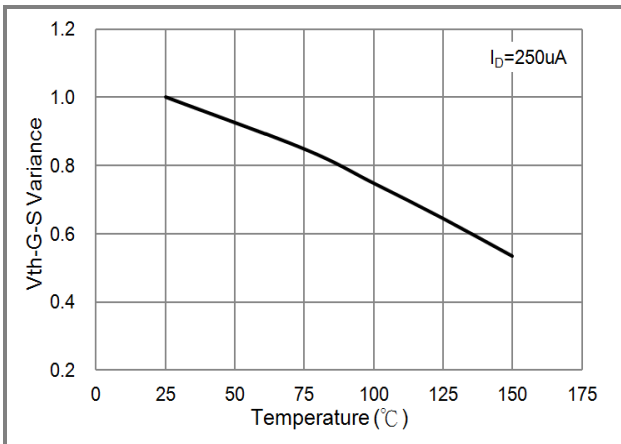


Fig.9 Threshold Voltage Variation with Temperature

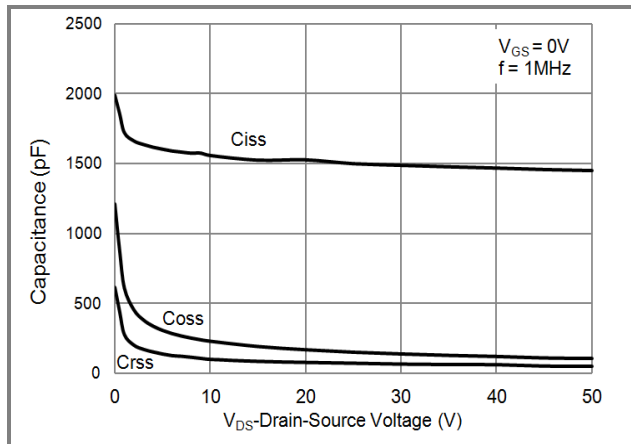


Fig.10 Capacitance vs. Drain-Source Voltage

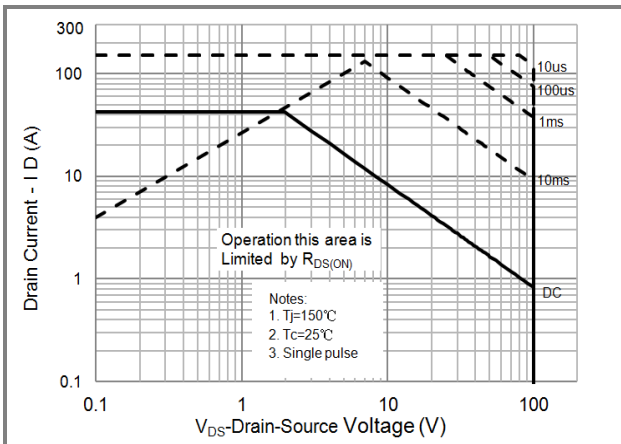


Fig.11 Maximum Safe Operating Area



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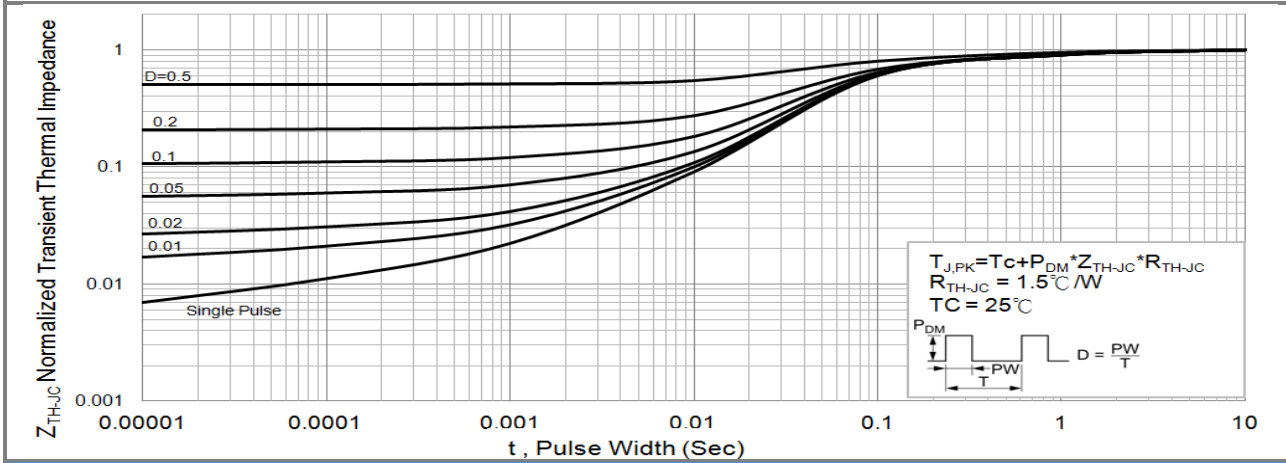


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width





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