

PJQ54813A-AU

80V P-Channel Enhancement Mode MOSFET

Voltage

-80 V

Current

-13 A

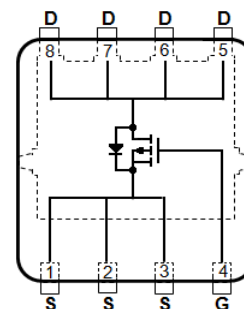
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-10A < 122m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-6A < 143m\Omega$
- 100% UIS tested
- Reliable and Rugged
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

DFN5060-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^{\circ}C$	I_D	-13	A
	$T_C=100^{\circ}C$		-9	
Pulsed Drain Current ^(Note 1)	$T_C=25^{\circ}C$	I_{DM}	-24	
Power Dissipation	$T_C=25^{\circ}C$	P_D	46	W
	$T_C=100^{\circ}C$		23	
Continuous Drain Current ^(Note 4)	$T_A=25^{\circ}C$	I_D	-3.5	A
	$T_A=70^{\circ}C$		-2.9	
Power Dissipation	$T_A=25^{\circ}C$	P_D	3.3	W
	$T_A=70^{\circ}C$		2.3	
Single Pulse Avalanche Current ^(Note 5)		I_{AS}	-8.4	A
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	35	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^{\circ}C$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	3.25	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	45	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

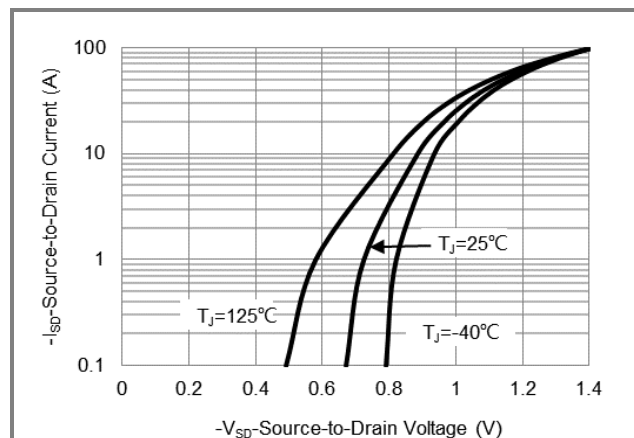
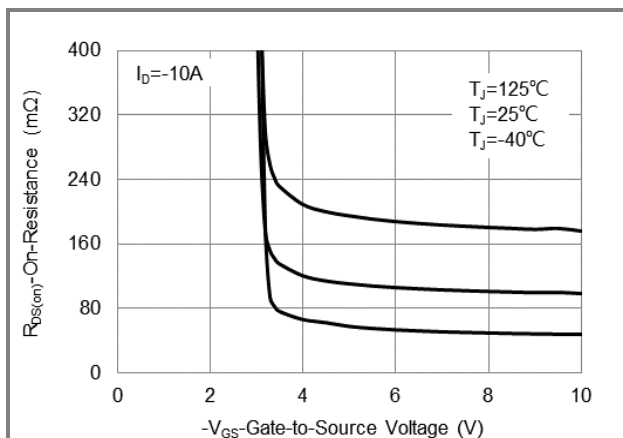
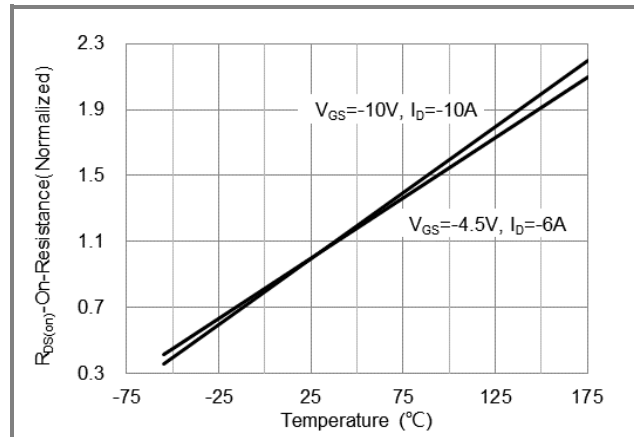
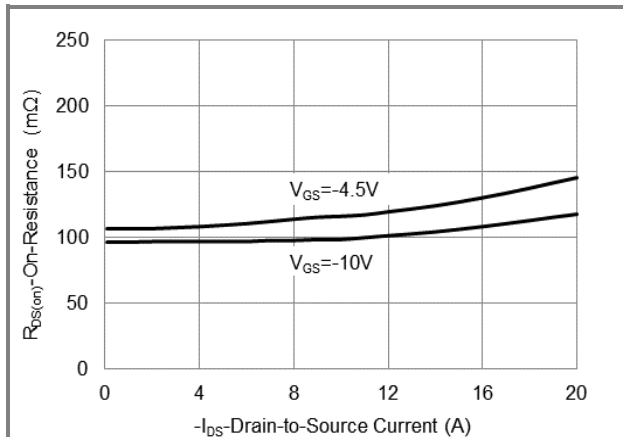
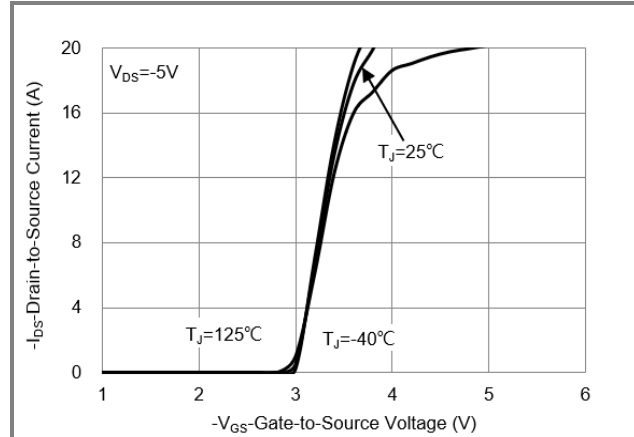
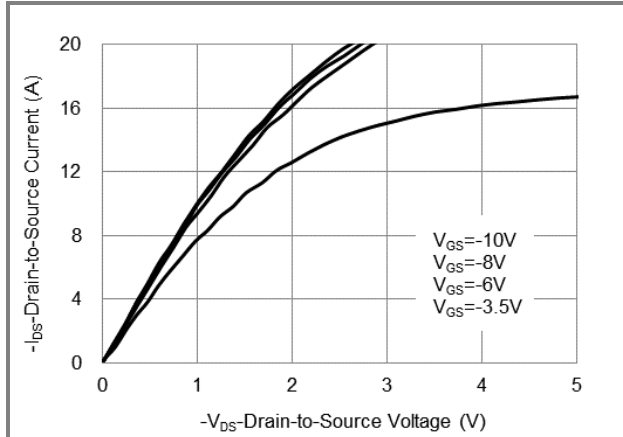
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-80	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.2	-1.7	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-10A	-	98	122	mΩ
		V _{GS} =-4.5V, I _D =-6A	-	110	143	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-80V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Q _g	V _{DS} =-40V, I _D =-10A, V _{GS} =-10V	-	21	28	nC
Gate-Source Charge	Q _{gs}		-	3.8	-	
Gate-Drain Charge	Q _{gd}		-	3.5	-	
Input Capacitance	C _{iss}	V _{DS} =-40V, V _{GS} =0V, f=1MHz	-	1151	1500	pF
Output Capacitance	C _{oss}		-	48	96	
Reverse Transfer Capacitance	C _{rss}		-	34	68	
Gate resistance	R _g	f=1MHz	-	10	-	Ω
Turn-On Delay Time	td _(on)	V _{DS} =-40V, I _D =-10A, V _{GS} =-10V, R _G =3Ω (Note 2)	-	5.1	-	ns
Turn-On Rise Time	tr		-	3.8	-	
Turn-Off Delay Time	td _(off)		-	38	-	
Turn-Off Fall Time	tf		-	16	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C (Package Limit)	-	-	-13	A
Pulsed Diode Forward Current	I _{SM}		-	-	-24	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V	-	-1	-1.3	V
Reverse Recovery Time	T _{rr}	V _{DD} =-40V,V _{GS} =0V,	-	18	-	ns
Reverse Recovery Charge	Q _{rr}	I _S =-10A,dI _S /dt=100A/us	-	14	-	nC

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=-8.4A, V_{DD}=-30V, V_{GS}=-10V. 100% test at L=0.5mH, I_{AS}=-8.8A in production.
6. Guaranteed by design, not subject to production testing.

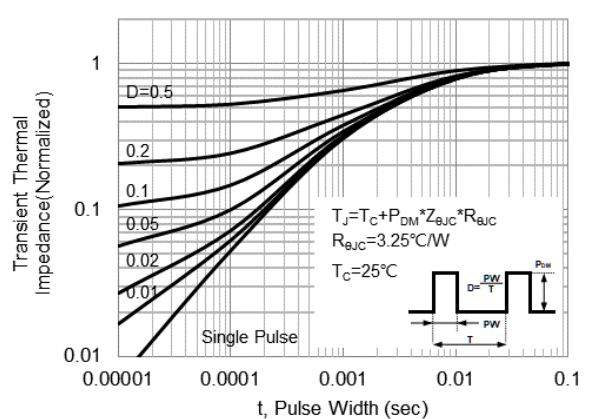
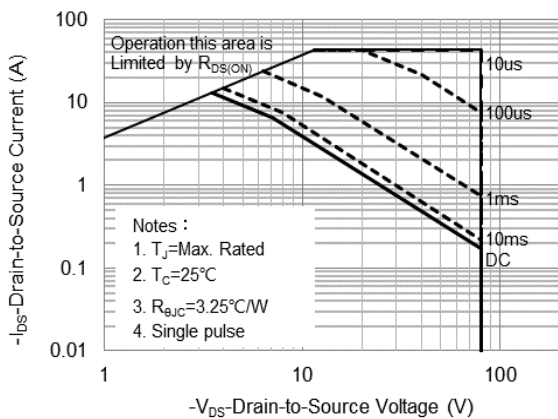
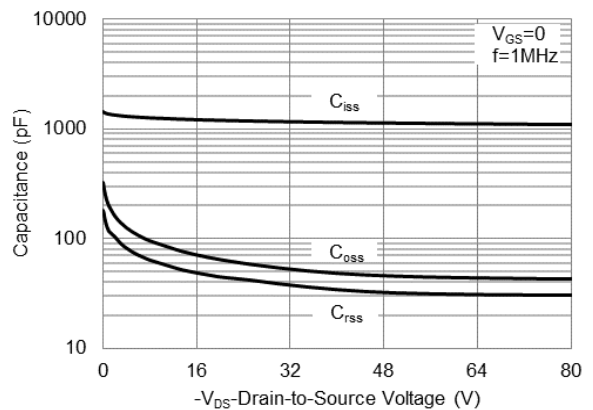
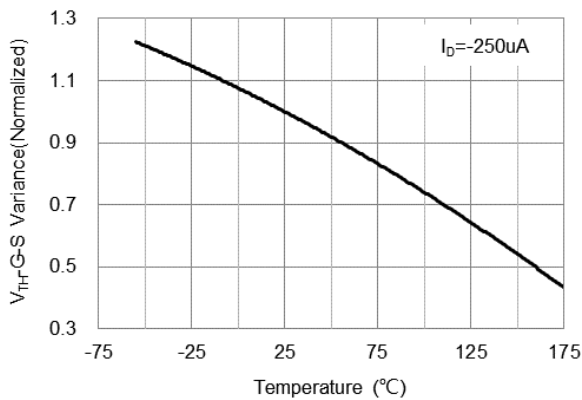
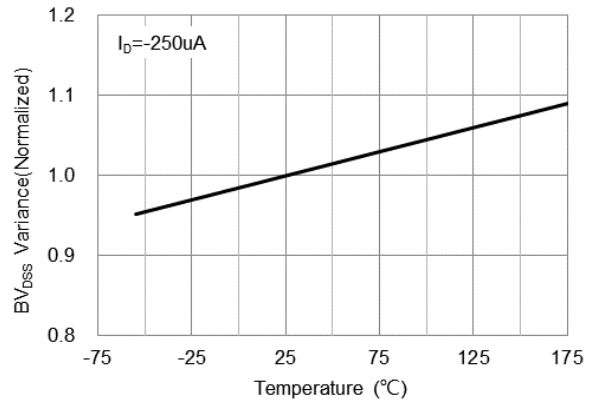
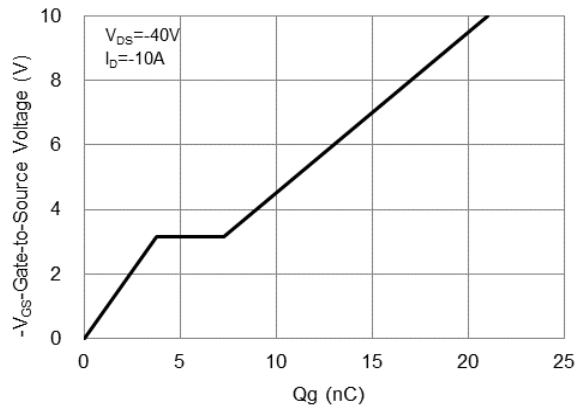
PJQ54813A-AU

TYPICAL CHARACTERISTIC CURVES



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TYPICAL CHARACTERISTIC CURVES



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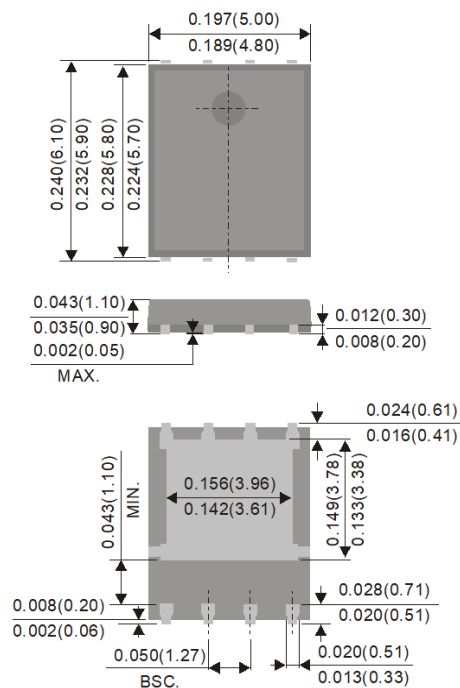
Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ54813A-AU	DFN5060-8L	3K pcs / 13" reel	Q54813A

Packaging Information & Mounting Pad Layout

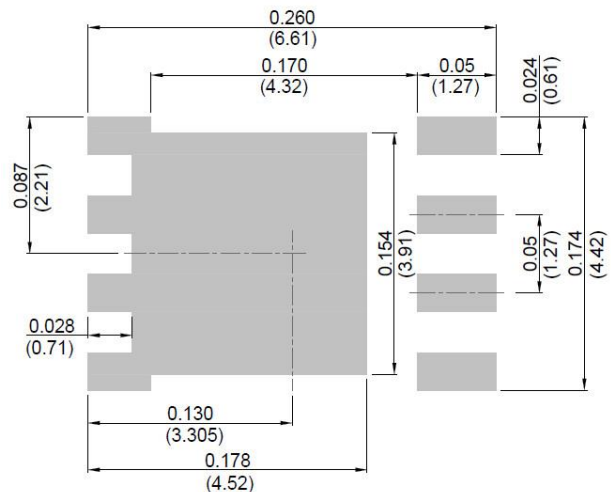
DFN5060-8L Dimension

Unit: inch(mm)



DFN5060-8L Pad Layout

Unit: inch(mm)



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