

PJQ44815AP-AU

80V P-Channel Enhancement Mode MOSFET

Voltage

-80 V

Current

-10 A

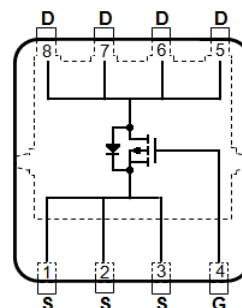
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-5A < 170m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-2A < 200m\Omega$
- 100% UIS tested
- Reliable and Rugged
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ\text{C}$	I_D	-10	A
	$T_C=100^\circ\text{C}$		-7	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	-18	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	36.6	W
	$T_C=100^\circ\text{C}$		18.3	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	-2.6	A
	$T_A=70^\circ\text{C}$		-2.2	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.5	W
	$T_A=70^\circ\text{C}$		1.8	
Single Pulse Avalanche Current ^(Note 5)		I_{AS}	-6.3	A
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	20	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	4.1	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	60	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

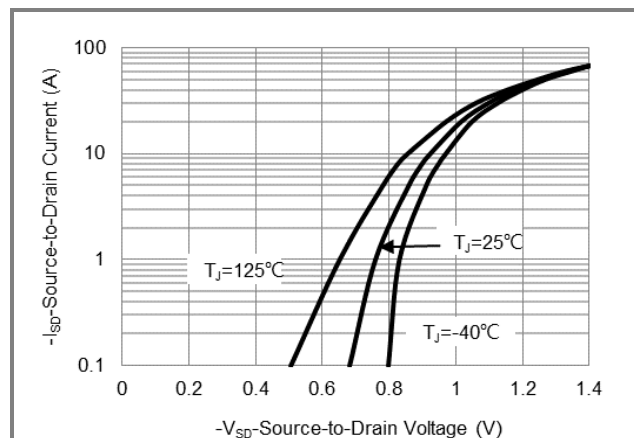
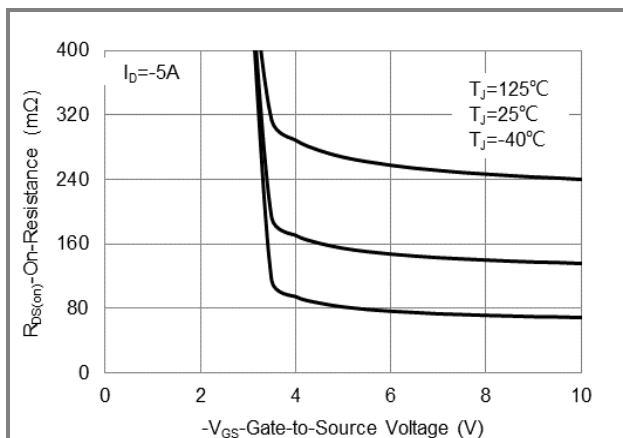
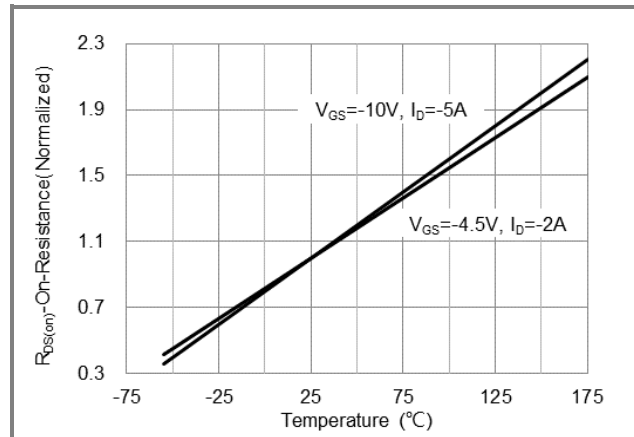
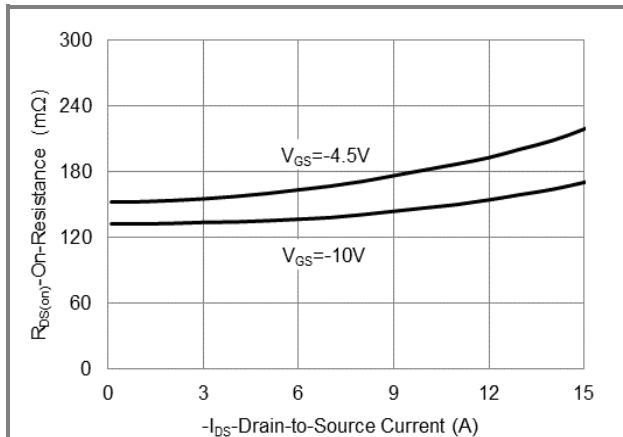
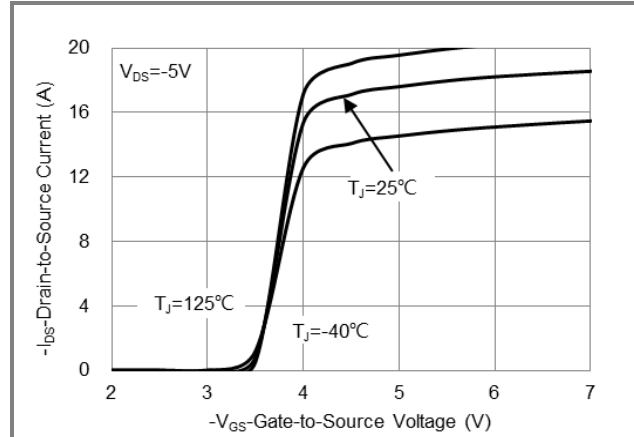
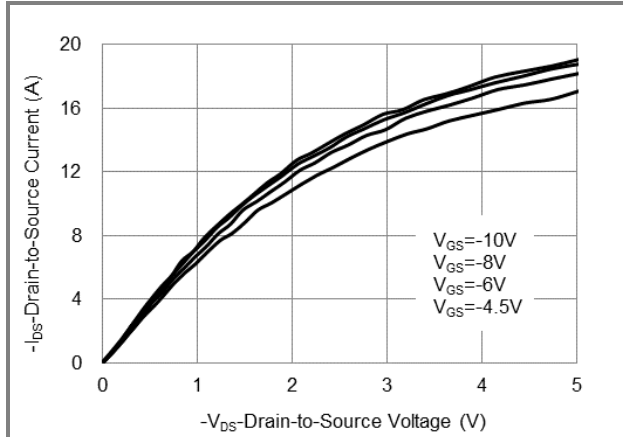
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-80	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.2	-1.7	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-5A	-	136	170	mΩ
		V _{GS} =-4.5V, I _D =-2A	-	154	200	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-80V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Q _g	V _{DS} =-40V, I _D =-5A, V _{GS} =-10V	-	16.3	22	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	
Gate-Drain Charge	Q _{gd}		-	2.9	-	
Input Capacitance	C _{iss}	V _{DS} =-40V, V _{GS} =0V, f=1MHz	-	848	1200	pF
Output Capacitance	C _{oss}		-	37	74	
Reverse Transfer Capacitance	C _{rss}		-	26	52	
Gate resistance	R _g	f=1MHz	-	13	-	Ω
Turn-On Delay Time	td _(on)	V _{DS} =-40V, I _D =-5A, V _{GS} =-10V, R _G =3Ω (Note 2)	-	4.7	-	ns
Turn-On Rise Time	tr		-	3.7	-	
Turn-Off Delay Time	td _(off)		-	34	-	
Turn-Off Fall Time	tf		-	15	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25 ^o C (Package Limit)	-	-	-10	A
Pulsed Diode Forward Current	I _{SM}		-	-	-18	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V	-	-1	-1.3	V
Reverse Recovery Time	Trr	V _{DD} =-40V,V _{GS} =0V	-	18	-	ns
Reverse Recovery Charge	Qrr	I _S =-5A,dI _S /dt=100A/us	-	15	-	nC

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=4.1°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=-6.3A, V_{DD}=-30V, V_{GS}=-10V. 100% test at L=0.5mH, I_{AS}=-6.5A in production.
6. Guaranteed by design, not subject to production testing.

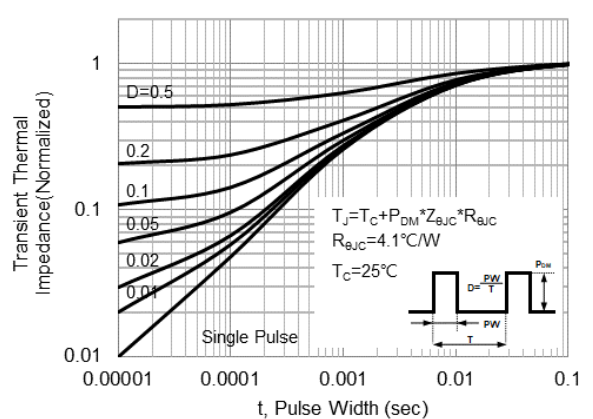
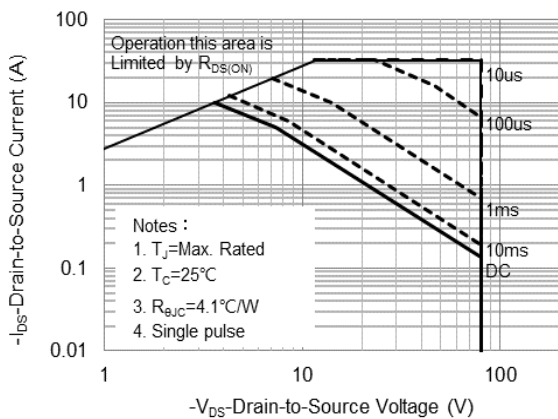
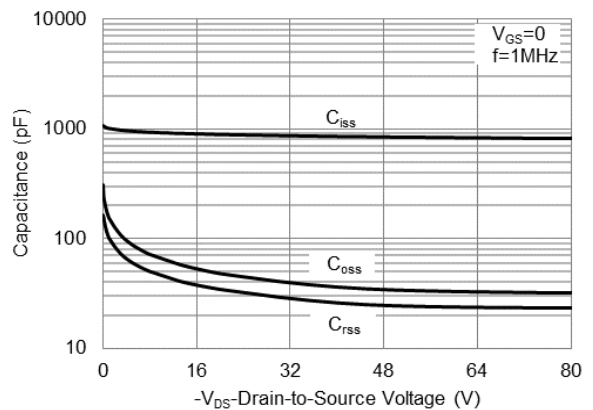
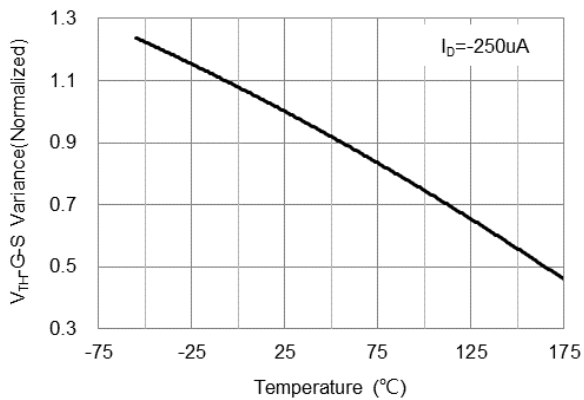
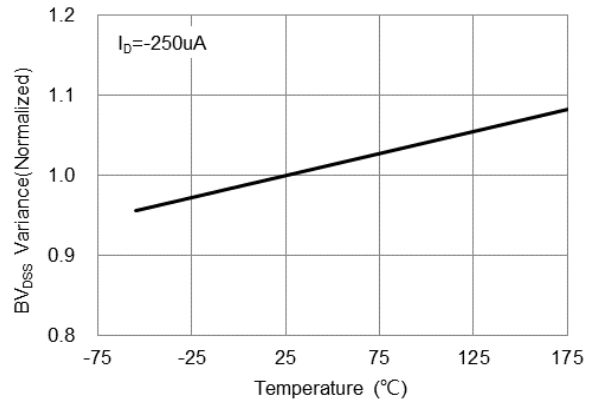
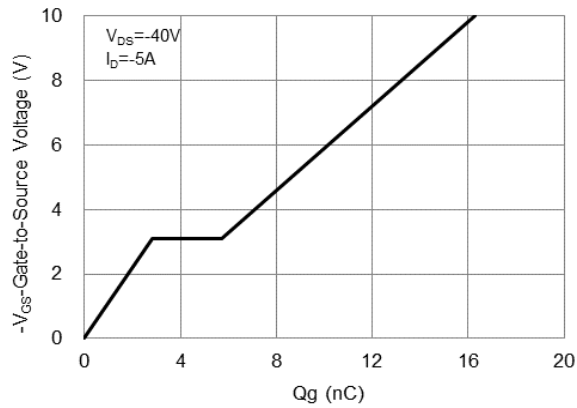
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TYPICAL CHARACTERISTIC CURVES



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TYPICAL CHARACTERISTIC CURVES

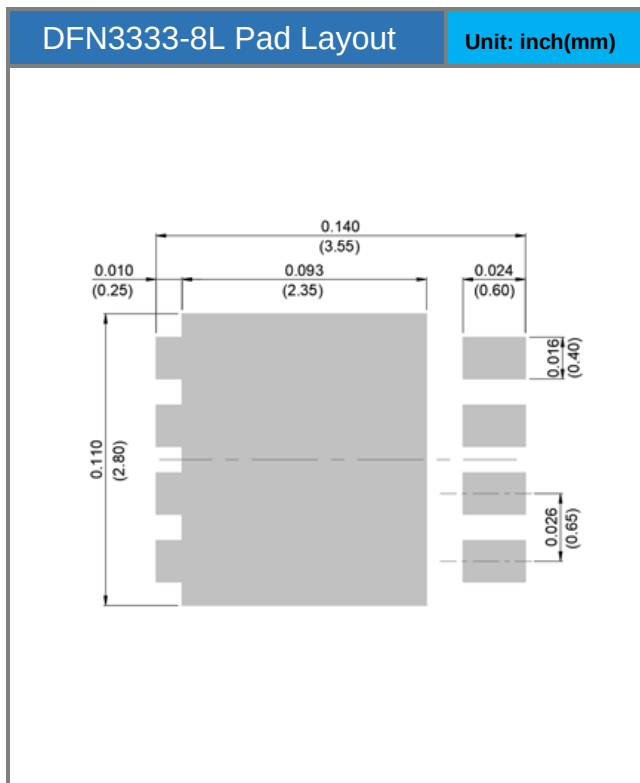
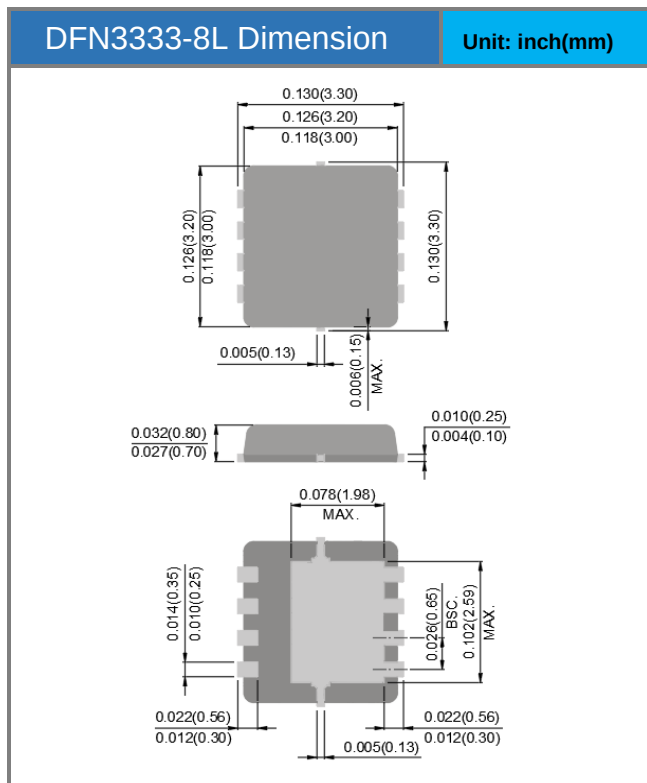


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ44815AP-AU	DFN3333-8L	5K pcs / 13" reel	44815A

Packaging Information & Mounting Pad Layout



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