12-Bit, 8-Ch ADC and Temperature Sensor System Monitor with I²C Interface

Description

The PJ79818 is a system monitor chip with I²C interface.

The PJ79818 include a local temperature sensor, 8-channel analog input. An onboard temperature sensor, combined with WATCHDOG window comparators, and an interrupt output pin $\overline{INT}$ allow easy monitoring and out-of-range alarms for every channel. A high performance internal reference is also available to provide for a complete solution in the most difficult operating conditions.

Analog input can be used for voltage monitor, like connecting analog output temperature sensor or monitor power supply voltage.

The PJ79818 supports standard mode (100kHz) and fast mode (400kHz) I²C interface.

Available Package: TSSOP-16P package.

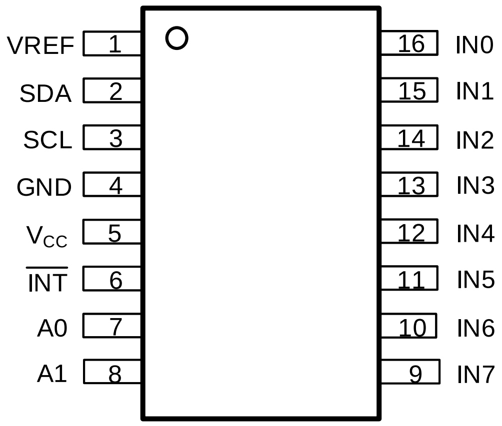
Features

- Operation Voltage: 3V to 5.5V
- 12Bit Resolution Delta-Sigma ADC
- Local Temperature Accuracy:
  (-25℃ to 100℃) ±1℃(Max.)
  (-40℃ to 125℃) ±1.5℃(Max.)
- 2.56V Internal V_{REF} or Variable External V_{REF}
- WATCHDOG Window Comparators with Status and Mask Registers of All Measured Values
- Independent Registers for Storing Measured Values
- $\overline{INT}$ Output Notifies Microprocessor of Error Event
- I²C/SMBus Serial Bus Interface Compatibility
  - ✓ 9 Selectable Addresses
  - ✓ TIME-OUT Reset Function to Prevent I²C Bus Lock-Up
- Individual Channel Shutdown to Limit Power Consumption
- Deep Shutdown Mode to Minimize Power Consumption
- Temperature Range: -40℃ to 125℃

Applications

- Communications Infrastructure
- Thermal and Hardware Server Monitors
- System Monitors
- Industrial and Medical Systems

Pin Configurations



TSSOP-16P

Typical Application

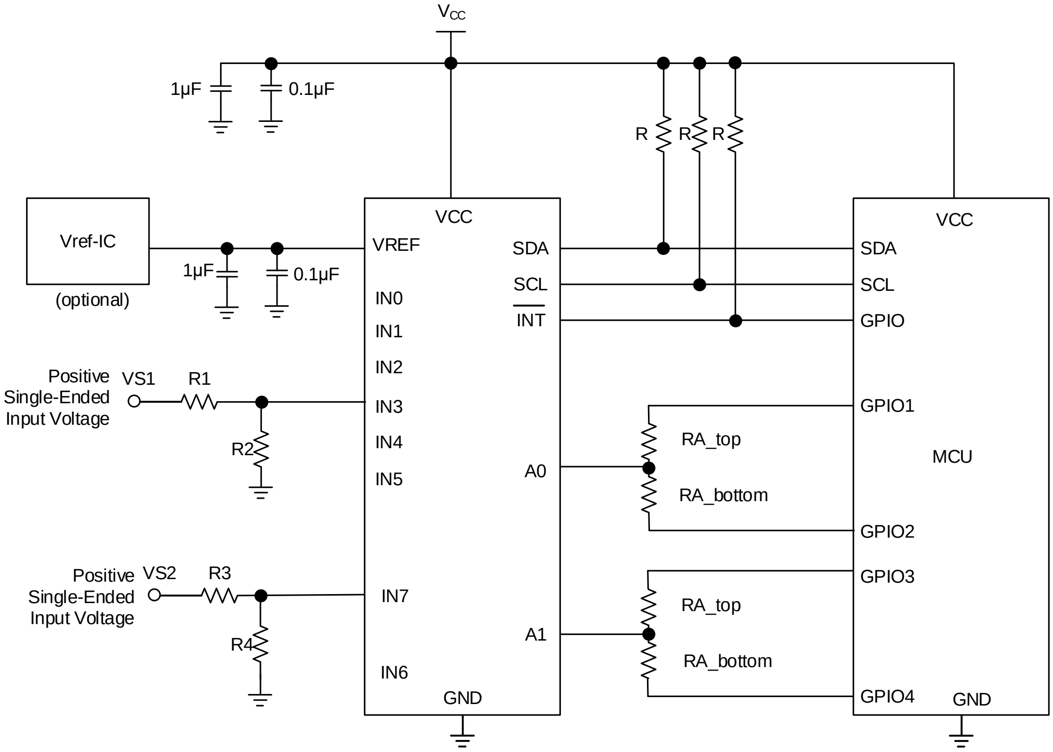


Figure 1 Typical Application of PJ79818

Pin Description

PIN Name	PIN No.	Description
	TSSOP-16P	
V_{REF}	1	ADC external reference. PJ79818 allows two choices for sourcing V_{REF}: Internal or External. If the 2.56V internal V_{REF} is used, leave this pin unconnected. If the external V_{REF} is used, source this pin with a voltage between 1.25V and V_{CC}. At Power-On-Reset (POR), the default setting is the internal V_{REF}. Bypass with the parallel combination of 1μF (electrolytic or tantalum) and 0.1μF (ceramic) capacitors.
SDA	2	Serial Bus Bidirectional Data. NMOS open-drain output. Requires external pull-up resistor to function properly.
SCL	3	Serial Bus Clock. Requires external pull-up resistor to function properly.
GND	4	Power Ground. Internally connected to all of the circuitry.
VCC	5	3.0V to 5.5V power. Bypass with the parallel combination of 1μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
$\overline{\text{INT}}$	6	Interrupt Request. Active Low, NMOS, open-drain. Requires external pull-up resistor to function properly.
A0	7	Tri-Level Serial Address pins that allow 9 devices on a single I^2C bus.
A1	8	Tri-Level Serial Address pins that allow 9 devices on a single I^2C bus.
IN7	9	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN6	10	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN5	11	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN4	12	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN3	13	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN2	14	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN1	15	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.
IN0	16	The full scale range will be controlled by the internal or external V_{REF}. This input can only be assigned as single-ended.

Function Block

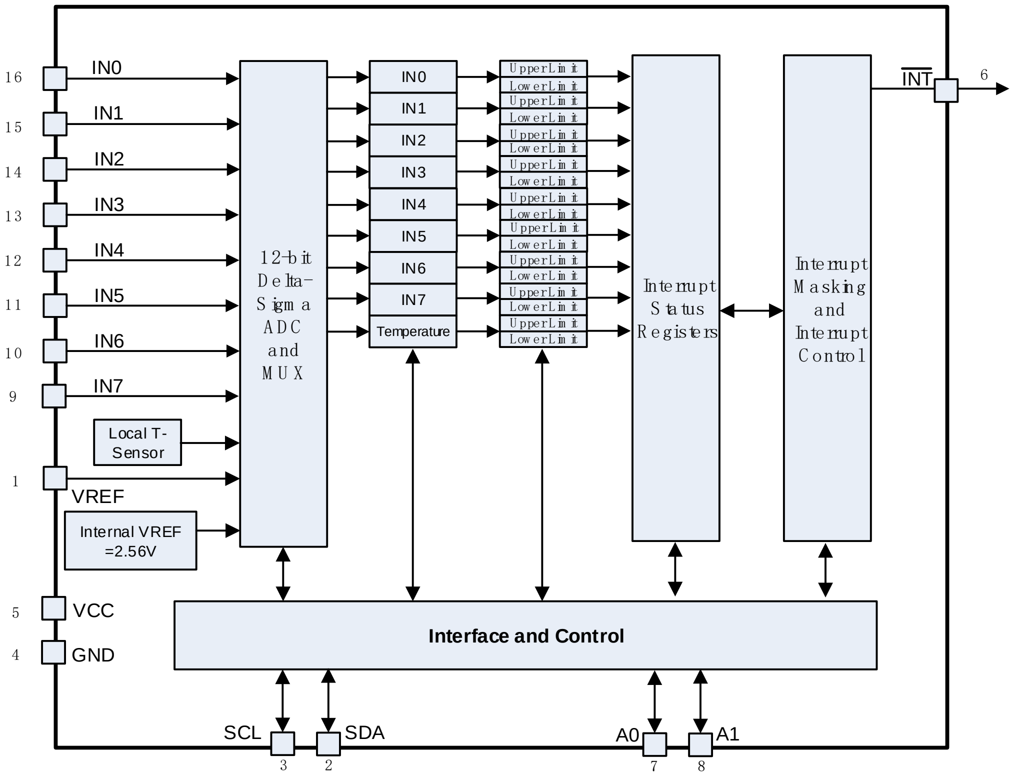


Figure 2 PJ79818 Function Block

Ordering Information

Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
PJ79818B	Halogen free	TSSOP-16P	PJ79818 BYMDNN	Tape & Reel	4,000	-40℃ ~ +125℃

Notes：
1. Panjit can meet RoHS2.0/REACH requirement. Most package types Panjit offers only states halogen free, instead of lead free.
2. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

Specification

Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} to GND	-0.3 to 6.0	V
SDA, SCL, A0, A1,$\overline{INT}$ Voltage		-0.3 to 6.0	V
IN0-IN7, V_{REF} Voltage		-0.3 to V_{CC}+0.3	V
Input Current at Any Pin[2]		±5	mA
Package Input Current		±30	mA
Storage temperature Range	T_{STG}	-65 to 150	℃
Maximum Junction Temperature	T_{JMAX}	150	℃
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	℃

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.
2. If the input voltage at any pin exceeds the power supply (that is, VIN < GND or VIN > VCC) but is less than the absolute maximum ratings, then the current at that pin must be limited to 5 mA. The 30 mA maximum package input current rating limits the number of pins that can safely exceed the power supply with an input current of 5 mA to six pins. Parasitic components and/or ESD protection circuitry are shown in the Pin Descriptions table.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-4	4	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-1	1	kV

1. Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
2. Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
3. Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	3		5.5	V
Voltage on SCL, SDA, A1, A0 , $\overline{INT}$		-0.05		5.5	V
Operation Temperature Range	T_A	-40		125	℃

Electrical Characteristics

Test Conditions: C_{IN} = 1uF&0.1uF, V_{CC} = 3V to 5.5V, unless otherwise specified. All limits are 100% tested at T_A=25℃.[1]

Parameter	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
Supply voltage	V_{CC}		3		5.5	V
V_{REF}	V_{REF}	External Reference Voltage	1.25		V_{CC}	V
		Internal Reference Voltage		2.56		V
				23		ppm/℃
Current in shutdown mode or deep shutdown mode	$I_{CC\_SHUTDOWN}$	Shutdown Mode, V_{CC} = 5.5V, -40~125℃		37	100	μA
		Shutdown Mode, V_{CC} = 3.6V, -40~125℃		20	80	μA
		Deep Shutdown Mode, V_{CC} = 5.5V, -40~125℃		2	10	μA
		Deep Shutdown Mode, V_{CC} = 3.6V, -40~125℃		1	5	μA
		Shutdown Mode, V_{CC} = 5.5V, -40~125℃		37	100	μA
Voltage Conversion Current	I_{CC_VOL}	V_{CC} = 3.6 V		130		μA
		V_{CC} = 5.5 V		120		μA
Temperature Conversion Current	I_{CC_TEMP}	V_{CC} = 3.6 V		140		μA
		V_{CC} = 5.5 V		130		μA
TEMPERATURE-to-DIGITAL CONVERTER CHARACTERISTICS						
Temperature Sensor Accuracy	T_{RAC}	T_A = -25 to 100℃	-1.0		1.0	℃
		T_A = -40 to 125℃	-1.5		1.5	℃
Resolution				0.0625		℃
Total Conversion time	t_{CON}	Continuous Conversion Mode Each Enabled Voltage Channel		15		ms
		Continuous Conversion Mode Internal Temperature Sensor		2		ms
		Low Power Conversion Mode Enabled Voltage Channel(s) and Internal Temperature Sensor		874		ms
ANALOG-to-DIGITAL CONVERTER CHARACTERISTICS						
Input Range	V_{IN}		0		2.560	V
Resolution		12 bit ADC, full scale 2.56V		0.625		mV
ADC bit				12		Bit

Electrical Characteristics (continued)

Parameter	Symbol	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Total Unadjusted Error[2]	TUE	Internal V_{REF}, Single-Ended, V_{CC} = 3V to 3.6V.	-40~125℃	-0.5		0.6	% of FS
		Internal V_{REF}, Single-Ended, V_{CC} = 4.5V to 5.5V					
		External V_{REF} = 1.25V, Single-Ended, V_{CC} = 3V to 3.6V.	-40~125℃	-0.6		0.1	% of FS
		External V_{REF} = 2.56V, Single-Ended, V_{CC} = 3.6V to 5.5V.					
Gain Error	GE	Internal V_{REF}, V_{CC} = 3V to 3.6V.	-40~125℃	-0.25		0.6	% of FS
		Internal V_{REF}, V_{CC} = 4.5V to 5.5V					
		External V_{REF} = 1.25V, V_{CC} = 3V to 3.6V.	-40~125℃	-0.45		0.2	% of FS
		External V_{REF} = 2.56V, V_{CC} = 4.5V to 5.5V.					
Offset Error	OE	External V_{REF} = 1.25V, Single-Ended, V_{CC} = 3V to 3.6V.	-40~125℃	-0.5		0.1	% of FS
		External V_{REF} = 2.56V, Single-Ended, V_{CC} = 4.5V to 5.5V					
ADC INPUT CHARACTERISTICS							
ON-Resistance[3]	R_{ON}				2		kΩ
			-40~125℃			10	kΩ
Input Current (On Channel Leakage Current) [3]	I_{ON}			-0.005		0.005	μA
Off Channel Leakage Current[3]	I_{OFF}			-0.005		0.005	μA
DIGITAL OUTPUTS: $\overline{INT}$							
Logical 0 Output Voltage	$V_{OUT(0)}$	I_{OUT} = 5.0mA at V_{CC}=4.5V, I_{OUT} = 3mA at V_{CC}= 3V	-40~125℃			0.4	V

OPEN DRAIN SERIAL BUS OUTPUT: SDA							
Logical 0 Output Voltage	$V_{OUT(0)}$	I_{OUT} = 3.0 mA at V_{CC}= 4.5V	-40~125℃			0.4	V
DIGITAL INPUTS: A0 and A1							
Logical 1 Input Voltage	$V_{IN(1)}$	-40~125℃		0.9*V_{CC}		5.5	V
Logical Middle Input Voltage	V_{IM}	-40~125℃		0.43*V_{CC}		0.57*V_{CC}	V
Logical 0 Input Voltage	$V_{IN(0)}$	-40~125℃		-0.05		0.1*V_{CC}	V

Electrical Characteristics (continued)

Parameter	Symbol	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SERIAL BUS INPUTS: SCL and SDA							
Logical 1 Input Voltage		$V_{IN(1)}$	-40~125℃	0.8*V_{CC}		5.5	V
Logical 0 Input Voltage		$V_{IN(0)}$	-40~125℃	-0.05		0.2*V_{CC}	V
ALL DIGITAL INPUTS: SCL, SDA, A0, A1							
Logical 1 Input Current	$I_{IN(1)}$	V_{IN} = V_{CC}			-0.005		µA
			-40~125℃	-1			µA
Logical 0 Input Current	$I_{IN(0)}$	V_{IN} = GND			0.005		µA
			-40~125℃			1	µA
Digital Input Capacitance[4]	C_{IN}				20		pF

Notes:

1. All typical values are at nominal supply voltage (3.3, or 5V VCC) and T_A = 25℃.
2. TUE(Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.
3. Limit is specified by design.
4. Limit is specified by design.

AC Electrical Characteristics[1]

Parameter	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL frequency	f_{SCL}	SCL pin[2]	10		400	kHz
Timeout of detecting clock or data low period time	t_{TOUT}		25		35	ms
Clock low period time	t_{LOW}		4.7			µs
Clock high period time	t_{HIGH}		4.0		50	µs
Bus free time	t_{BUF}	Between Stop and Start condition	4.7			µs
Hold time after Start condition	$t_{HD:STA}$		4.0			µs
Repeated Start condition setup time	$t_{SU:STA}$		4.7			µs
Stop condition setup time	$t_{SU:STO}$		4.0			µs
Data Hold time	$t_{HD:DAT}$		300			ns
Data Setup time	$t_{SU:DAT}$		250			ns
Clock/Data fall time	t_F				300	ns
Clock/Data rise time	t_R				1000	ns

Notes:
1. All devices are 100% production tested at T_A = +25℃; all specifications over the automotive temperature range is guaranteed by design, not production tested.
2. There is no minimal clock frequency limitation for I2C protocol; the minimal frequency is limited by time-out feature with 35ms in typical, we recommend the minimal frequency of clock is 10000Hz.

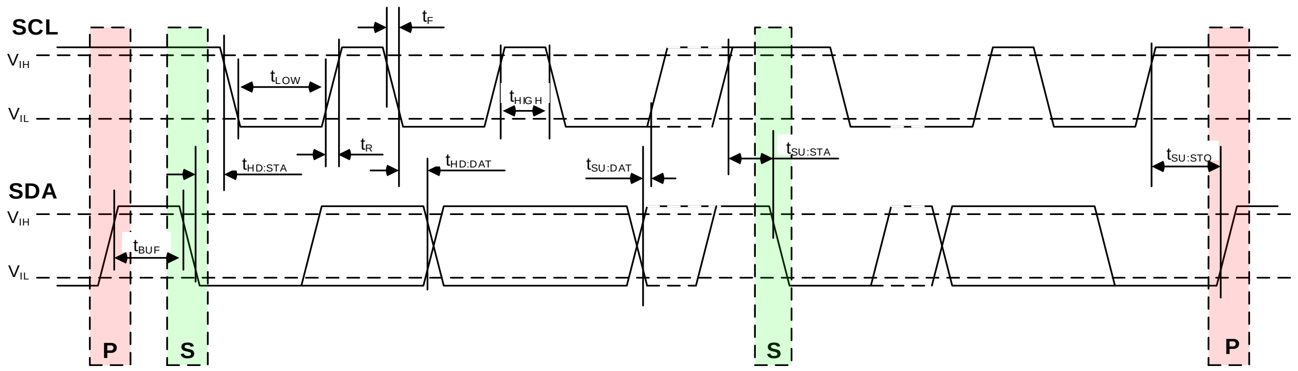


Figure 3 I^{2}C Timing Diagram

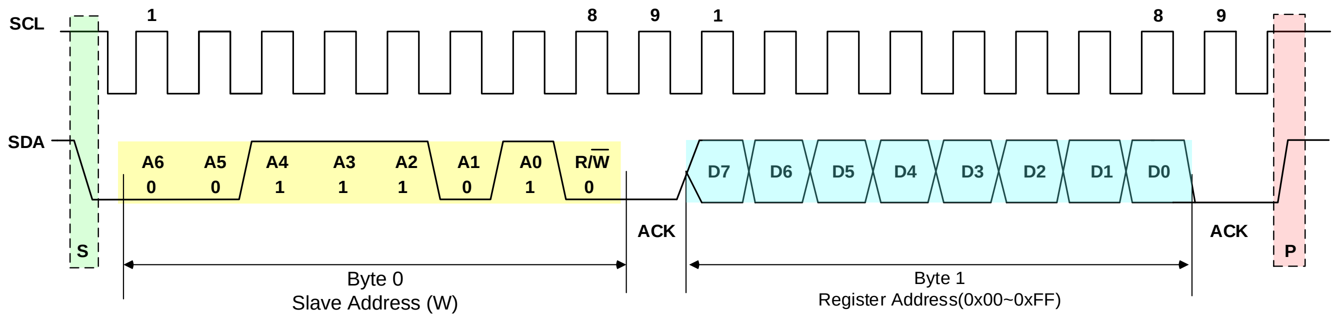


Figure 4 I^{2}C Write Timing Diagram (Internal Address register set only)

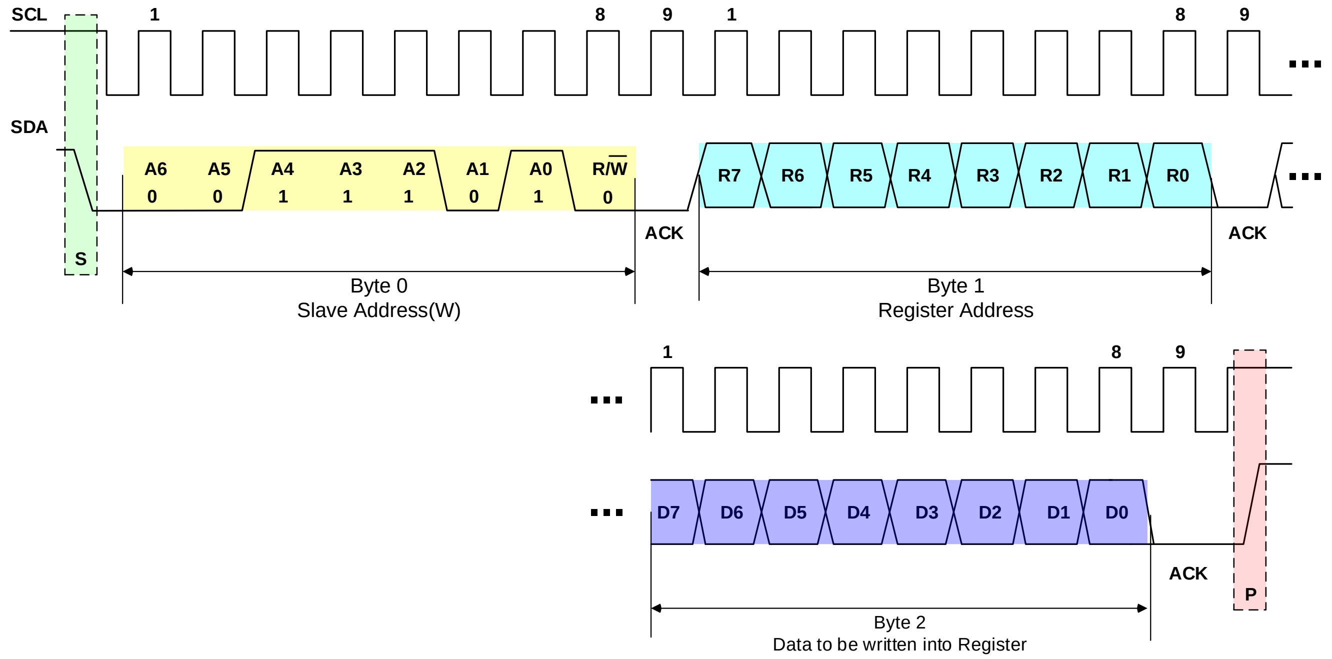


Figure 5 I^{2}C Write Timing Diagram (Internal Address register set with data byte write)

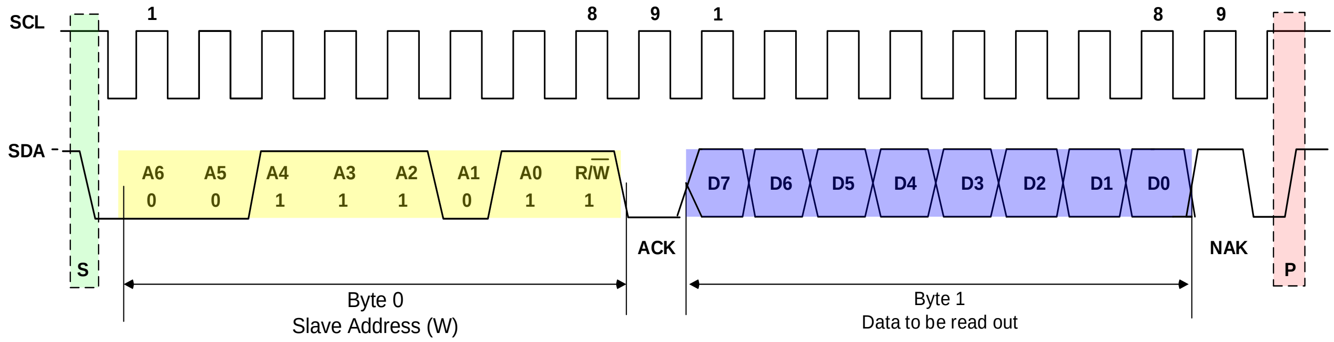


Figure 6 I^{2}C Read Timing Diagram (Single byte read with present internal address register)

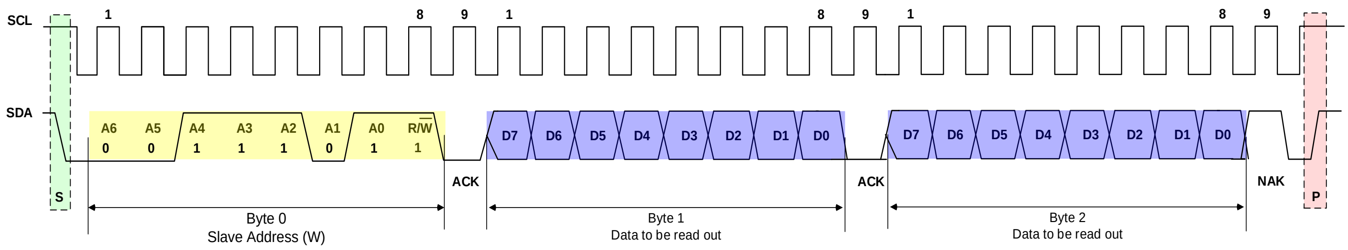


Figure 7 I^{2}C Read Timing Diagram (Double bytes read with present internal address register)

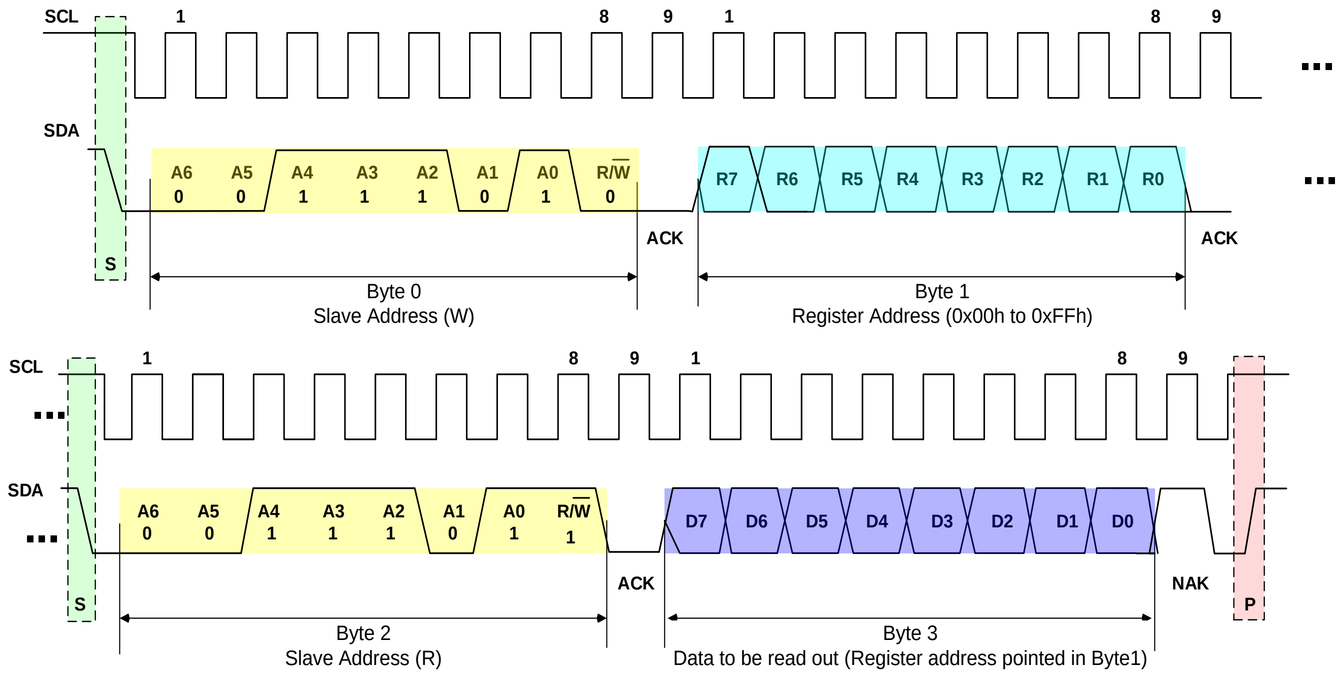


Figure 8 I^{2}C Read Timing Diagram (Single byte read with internal set using a Repeat Start)

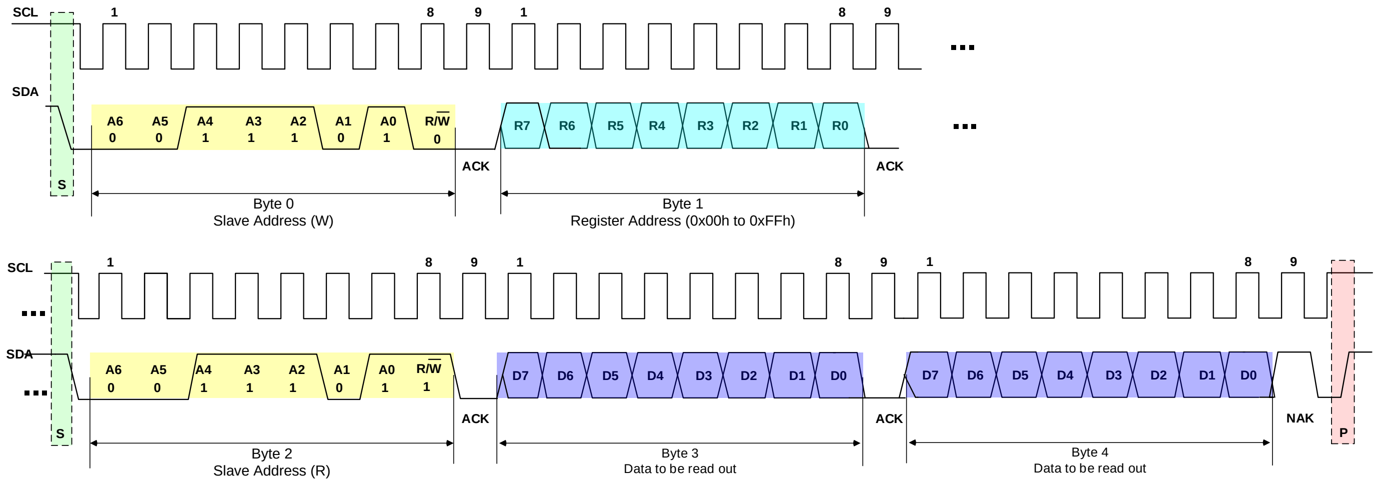


Figure 9 I^{2}C Read Timing Diagram (Double bytes read with internal set using a Repeat Start)

Function Descriptions

Overview

The PJ79818 provides 8 analog inputs, a temperature sensor, a delta-sigma ADC, an external or internal V_{REF} option, and WATCHDOG registers on a single chip. An I²C Serial Bus interface is also provided. The PJ79818 can perform voltage and temperature monitoring for a variety of systems.

The PJ79818 continuously converts the voltage input to 12-bit resolution with an internal V_{REF} of 0.625mV LSb (Least Significant bit) weighting, yielding input range of 0V to 2.56V. There is also an external V_{REF} option that ranges from 1.25V to V_{CC}. The analog inputs are intended to be connected to several power supplies present in a variety of systems. All eight channel inputs are single-ended. Temperature can be converted to a 12-bit two's complement word with resolutions of 0.0625℃ per LSb. The PJ79818 provides a number of internal registers. These registers are summarized in Table 4.

The PJ79818 supports Standard Mode (SM, 100kbps) and Fast Mode (FM, 400kbps) I²C interface modes of operation. PJ79818 includes an analog filter on the I²C digital control lines that allows improved noise immunity. The device also supports TIME-OUT reset function on SDA and SCL to prevent I²C bus lock-up. Two tri-level address pins allow up to 9 devices on a single I²C bus.

At start-up, PJ79818 cycles through each measurement in sequence and continuously loops through the sequence based on the Conversion Rate Register (address 0x07) setting. Each measured value is compared to values stored in the Limit Registers (addresses 0x2A-0x39). When the measured value violates the programmed limit, the PJ79818 will set a corresponding interrupt bit in the Interrupt Status Registers (address 0x01). An interrupt output pin, INT, is also available and fully programmable.

Supply Voltage (V_{CC})

The PJ79818 operates with a supply voltage (V_{CC}) that has a range between 3V to 5.5V. Take care to bypass this pin with a parallel combination of 1µF (electrolytic or tantalum) capacitor and 0.1µF (ceramic) bypass capacitor.

Voltage References (V_{REF})

The reference voltage (V_{REF}) sets the analog input range. The PJ79818 has two options for setting V_{REF}. The first option is to use the internal V_{REF}, which is equal to 2.56V. The second option is to source V_{REF} externally through pin 1 of PJ79818. In this case, the external V_{REF} will operate in the range of 1.25V to V_{CC}. The default V_{REF} selection is the internal V_{REF}. If the external V_{REF} is preferred, use the Advanced Configuration Register - Address 0x0B to change this setting.

V_{REF} source must have low output impedance and needs to be bypassed with a minimum capacitor value of 0.1µF. A larger capacitor value of 1µF placed in parallel with the 0.1µF is preferred. V_{REF} of the PJ79818, like all ADC converters, does not reject noise or voltage variations. Keep this in mind if V_{REF} is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will show in the digital results.

Analog Inputs (IN0 - IN7)

The 79818 allows up to 8 single-ended inputs as selected by the modes of operation. The input types are described in the next subsections.

Single-Ended Input

PJ79818 allows a maximum of 8 single-ended inputs, where the source's voltage is connected to INx ($0 \leq x \leq 7$). The source’s ground must be connected to PJ79818’s GND pin. In theory, INx can be of any value between 0V and (V_{REF}-3LSb/2), where LSb = $V_{REF}/2^{12}$.

To use the device single-endedly, refer to the Modes of Operation section and to bits1 of the Advanced Configuration Register - Address 0x0B. Figure 10 shows the appropriate configuration for a single-ended connection.

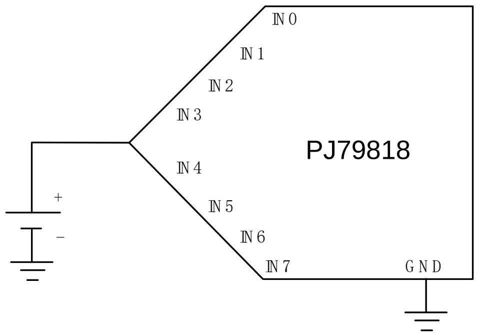


Figure 10 Single-Ended Configuration

Device Functional Modes

Modes of Operation

PJ79818 allows 2 modes of operation, as summarized in the following table. Set the desired mode of operation using the Advanced Configuration Register - Address 0Bh, bits 1).

Table 1 Modes of Operation

CH.	Mode0	Mode1
1	IN0	IN0
2	IN1	IN1
3	IN2	IN2
4	IN3	IN3
5	IN4	IN4
6	IN5	IN5
7	IN6	IN6
8	NC	IN7
Local Temperature	Yes	No

Programming

Interface

The Serial Bus control lines include the SDA (serial data), SCL (serial clock), and A0-A1 (Serial Bus Address) pins. The PJ79818 can only operate as a slave. The SCL line only controls the serial interface, and all of other clock functions within PJ79818 are done with a separate asynchronous internal clock.
When the Serial Bus Interface is used, a write will always consists of the PJ79818 Serial Bus Address byte, followed by the Register Address byte, then the Data byte. Figure 4 and Figure 5 are two examples showing how to write to the PJ79818.

There are two cases for a read:
1. If the Register Address is known to be at the desired address, simply read the PJ79818 with the Serial Bus Address byte, followed by the Data byte read from the PJ79818.
2. If the Register Address value is unknown, write to the PJ79818 with the Serial Bus Address byte, followed by the desired Register Address byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Address byte, followed by the Data byte read from the PJ79818.
The Serial Bus Address can be found in the next section, and the Register Address can be found in Register Maps.

I²C Bus Address

There are nine different configurations for the PJ79818 Serial Bus Address, thus nine devices are allowed on a single I²C bus. Examples to set each address bit low, high, or to midscale can be found in Typical Application. The Serial Bus Address can be set as follows:

Table 2 Serial Bus Address Table

A1	A0	Serial Bus Address [A6][A5][A4]…[A0]	SERIAL BUS ADDRESS (HEX)
Low	Low	001_1101b	0x1D
Low	Mid	001_1110b	0x1E
Low	High	001_1111b	0x1F
Mid	Low	010_1101b	0x2D
Mid	Mid	010_1110b	0x2E
Mid	High	010_1111b	0x2F
High	Low	011_0101b	0x35
High	Mid	011_0110b	0x36
High	High	011_0111b	0x37

Time-out

The PJ79818 I²C state machine resets to its idle state if either SCL or SDA is held low for longer than 35ms. This feature also ensures that PJ79818 will automatically release SDA after driving it low continuously for 25 to 35ms, hence preventing I²C bus lock-up.

Register Maps

PJ79818 Internal Registers

Table 3 PJ79818 Internal Registers

Register Address	Register Name	Attribution	Default Value	REGISTER FORMAT	Register DESCRIPTION
0x00	Configuration Register	R/W	0x08	8-bit	Provides control and configuration
0x01	Interrupt Status Register	R	0x00	8-bit	Provides status of each WATCHDOG limit or interrupt event
0x03	Interrupt Mask Register	R/W	0x00	8-bit	Masks the interrupt status from propagating to $\overline{INT}$
0x07	Conversion Rate Register	R/W	0x00	8-bit	Controls the conversion rate
0x08	Channel Disable Register	R/W	0x00	8-bit	Disables conversion for each voltage or temperature channel
0x09	One-Shot Register	W	0x00	8-bit	Initiates a single conversion of all enabled channels
0x0A	Deep Shutdown Register	R/W	0x00	8-bit	Enables deep shutdown mode
0x0B	Advanced Configuration Register	R/W	0x00	8-bit	Selects internal or external V_{REF} and modes of operation
0x0C	Busy Status Register	R	0x02	8-bit	Reflects chip 'Busy' and 'Not Ready' statuses
0x20-0x27	Channel Readings Registers	R	---	16-bit	Report the channels (voltage or temperature) readings
0x2A-0x39	Limit Registers	R/W	---	8-bit	Set the limits for the voltage and temperature channels
0x3E	Manufacturer ID Register	R	0x59	8-bit	Reports the manufacturer's ID
0x3F	Revision ID Register	R	0x01	8-bit	Reports the revision's ID

Configuration Register - 0x00

Table 4 Address 0x00

Register Address 0x00	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Initialization	Reserved	Reserved	Reserved	$\overline{INT}$_Clear	Reserved	$\overline{INT}$_Enable	START
Default Value	0	0	0	0	1	0	0	0
Attribution	R/W	R	R	R	R/W	R	R/W	R/W

BIT	Name	Description
0	Start	0: PJ79818 in shutdown mode 1: Enable startup of monitoring operations
1	$\overline{INT}$_Enable	1: Enable the interrupt output pin, $\overline{INT}$
2	Reserved	
3	$\overline{INT}$_Clear	1: Clear the interrupt output pin, $\overline{INT}$, and the contents of Interrupt Status Registers. When this bit is set high, the device will continue the round-robin monitoring loop.
4-6	Reserved	

7	Initialization	1: Restore default values to the following registers: Configuration, Interrupt Status, Interrupt Mask, Conversion Rate, Channel Disable, One-Shot, Deep Shutdown, Advanced Configuration, Busy Status, Channel Readings, Limit, Manufacturer ID, Revision ID. This bit clears itself

The Configuration Register (address 00h) provides all control to the PJ79818. After POR, the 'START' bit (bit 0) is set low and the '$\overline{\text{INT}}$_Clear' bit (bit 3) is set high.

The Configuration Register has the ability to start and stop the PJ79818, enable and disable the $\overline{\text{INT}}$ output, and set the registers to their default values.

• Bit 0, 'START', controls the monitoring loop of the PJ79818. After POR, set this bit high to start conversion. Setting this bit low stops the PJ79818 monitoring loop and puts the PJ79818 in shutdown mode; thus, reducing power consumption. Even though this bit is set low, serial bus communication is possible with any register in the PJ79818. After an interrupt occurs, the INT pin will not be cleared if the user sets this bit low.

• Bit 1, '$\overline{\text{INT}}$_Enable', enables the interrupt output pin ($\overline{\text{INT}}$) when this bit is set high.

• Bit 3, '$\overline{\text{INT}}$_Clear', clears the interrupt output pin ($\overline{\text{INT}}$) and Interrupt Status Register (address 01h) when this bit is set high. When this bit is set high, the PJ79818 monitoring function will continue.

• Bit 7, 'INITIALIZATION', accomplishes the same function as POR, that is, it initializes all the registers to their default values when this bit is set high. This bit automatically clears after being set high.

Interrupt Status Register - 0x01

Table 5 Address 0x01

Register Address 0x01	**BIT7**	**BIT6**	**BIT5**	**BIT4**	**BIT3**	**BIT2**	**BIT1**	**BIT0**
Mode 0								
Definition	Hot Temperature Error	IN6_Error	IN5_Error	IN4_Error	IN3_Error	IN2_Error	IN1_Error	IN0_Error
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R
Mode 1								
Definition	IN7_Error	IN6_Error	IN5_Error	IN4_Error	IN3_Error	IN2_Error	IN1_Error	IN0_Error
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R

BIT	**Name**	**Description**
Mode 0		
0	IN0_Error	1: A High or Low limit has been exceeded
1	IN1_Error	1: A High or Low limit has been exceeded
2	IN2_Error	1: A High or Low limit has been exceeded
3	IN3_Error	1: A High or Low limit has been exceeded
4	IN4_Error	1: A High or Low limit has been exceeded

5	IN5_Error	1: A High or Low limit has been exceeded
6	IN6_Error	1: A High or Low limit has been exceeded
7	Hot Temperature Error	1: A High limit has been exceeded
Mode 1		
0	IN0_Error	1: A High or Low limit has been exceeded
1	IN1_Error	1: A High or Low limit has been exceeded
2	IN2_Error	1: A High or Low limit has been exceeded
3	IN3_Error	1: A High or Low limit has been exceeded
4	IN4_Error	1: A High or Low limit has been exceeded
5	IN5_Error	1: A High or Low limit has been exceeded
6	IN6_Error	1: A High or Low limit has been exceeded
7	IN7_Error	1: A High or Low limit has been exceeded

Each bit in this read-only register indicates whether the voltage reading ≥ the voltage high limit or < the voltage low limit, or the temperature reading ≥ the temperature high limit. For example, if "IN0 High Limit" register (address 2Ah) were set to 2V and if IN0 reading (address 20h) were 2.56V, then bit 'IN0 Error' would be 1, indicating that the voltage high limit has been exceeded.

Interrupt Mask Register - 0x03

Table 6 Address 0x03

Register Address 0x03	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Mode 0								
Definition	Temperature Mask	IN6 Mask	IN5 Mask	IN4 Mask	IN3 Mask	IN2 Mask	IN1 Mask	IN0 Mask
Default Value	0	0	0	0	0	0	0	0
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 1								
Definition	IN7 Mask	IN6 Mask	IN5 Mask	IN4 Mask	IN3 Mask	IN2 Mask	IN1 Mask	IN0 Mask
Default Value	0	0	0	0	0	0	0	0
Attribution	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Mode 0		
0	IN0 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
1	IN1 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
2	IN2 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
3	IN3 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
4	IN4 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
5	IN5 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
6	IN6 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
7	Temperature Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$

Mode 1		
0	IN0 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
1	IN1 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
2	IN2 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
3	IN3 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
4	IN4 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
5	IN5 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
6	IN6 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$
7	IN7 Mask	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{\text{INT}}$

This register masks the interrupt status from propagating to the interrupt output pin ($\overline{\text{INT}}$). For example, if bit 'IN0 Mask' = 1, then the interrupt output pin, $\overline{\text{INT}}$, would not be pulled low even if an error event occurs at IN0.

Conversion Rate Register - 0x07

Table 7 Address 0x07

Register Address 0x07	**BIT7**	**BIT6**	**BIT5**	**BIT4**	**BIT3**	**BIT2**	**BIT1**	**BIT0**
Definition	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Conversion Rate
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R/W

BIT	**Name**	**Description**
0	Conversion Rate	Controls the conversion rate: 0: Low Power Conversion Mode 1: Continuous Conversion Mode Note: This register must only be programmed when the device is in shutdown mode, that is, when the 'START' bit of the 'Configuration Register' (address 00h) = 0
1-7	Reserved	

There are three options for controlling the conversion rate. The first option is called the Low Power Conversion Mode, where the device converts all of the enabled channels then enters shutdown mode. This process takes approximately 874ms to complete.

The second option is the Continuous Conversion Mode, where the device continuously converts the enabled channels, thus never entering shutdown mode. A voltage conversion takes 15ms, and a temperature conversion takes 2ms. For example, if operating in mode 0 and three voltage channels were enabled, then each round-robin monitor would take 47ms (3 x 15ms + 2ms) to complete. Use the "Channel Disable Register" (address 08h) to disable the desired channel(s).

The third option is called the One-Shot mode, which will be discussed in the next subsection.

Channel Disable Register - 0x08

Table 8 Address 0x08

Register Address 0x08	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Mode 0								
Definition	Temperature Disable	IN6 Disable	IN5 Disable	IN4 Disable	IN3 Disable	IN2 Disable	IN1 Disable	IN0 Disable
Default Value	0	0	0	0	0	0	0	0
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 1								
Definition	IN7 Disable	IN6 Disable	IN5 Disable	IN4 Disable	IN3 Disable	IN2 Disable	IN1 Disable	IN0 Disable
Default Value	0	0	0	0	0	0	0	0
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	Name	Description
Mode 0		
0	IN0 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
1	IN1 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
2	IN2 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
3	IN3 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
4	IN4 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
5	IN5 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
6	IN6 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
7	Temperature Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
Mode 1		
0	IN0 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
1	IN1 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
2	IN2 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.

3	IN3 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
4	IN4 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
5	IN5 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
6	IN6 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.
7	IN7 Disable	1: Conversions are skipped and disabled, Readings register will save the value of the last conversion, and error events will be suppressed.

One-Shot Register - 0x09

Table 9 Address 0x09

Register Address 0x09	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	One-Shot
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R

BIT	Name	Description
0	One-Shot	1: Initiate a single conversion and comparison cycle when the device is in shutdown mode or deep shutdown mode, after which the device returns to the respective mode that it was in.
1-7	Reserved	

The One-Shot register is used to initiate a single conversion and comparison cycle when the device is in shutdown mode or deep shutdown mode, after which the device returns to the respective mode it was in. The obvious advantage of using this mode is lower power consumption because the device is operating in shutdown or deep shutdown mode.

This register is not a data register, and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this registe

Deep Shutdown Register - 0x0A

Table 10 Address 0x0A

Register Address 0x0A	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Deep Shutdown Enable
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R/W

BIT	Name	Description
0	Deep Shutdown Enable	1: When 'START' = 0 (address 00h, bit 0), setting this bit high will place the device in deep shutdown mode
1-7	Reserved	

The PJ79818 can be placed in deep shutdown mode, thus reducing more power consumption. The procedures for deep shutdown entrance are:

1. Enter shutdown by setting the 'START' bit of the "Configuration Register' (address 00h, bit 0) to 0.
2. Enter deep shutdown by setting the 'DEEP SHUTDOWN' bit (address 0Ah, bit 0) to 1.
3. A one-shot conversion can be triggered by writing any values to register address 09h.

Deep Shutdown Exit Procedure:

1. Set the 'DEEP SHUTDOWN' bit to 0.

Advanced Configuration Register - 0x0B

Table 11 Address 0x0B

Register Address 0x0B	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Mode Select	External Reference Enable
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R/W	R/W

BIT	Name	Description
0	External Reference Enable	0: Selects the 2.56V internal V_{REF} 1: Selects the variable external V_{REF}
1	Mode Select	0: Mode 0 1: Mode 1
2-7	Reserved	

Busy Status Register - 0x0C

Table 12 Address 0x0C

Register Address 0x0C	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Not Ready	Busy
Default Value	0	0	0	0	0	0	1	0
Attribution	R	R	R	R	R	R	R	R

BIT	Name	Description
0	Busy	1: PJ79818 is converting
1	Not Ready	1: Waiting for the power-up sequence to end
2-7	Reserved	

Channel Readings Registers - 0x20 - 0x27

Table 13 Address 0x20 – 0x27

Register Address	0x27	0x26	0x25	0x24	0x23	0x22	0x21	0x20
Mode 0								
Definition	Temperature Reading	IN6 Reading	IN5 Reading	IN4 Reading	IN3 Reading	IN2 Reading	IN1 Reading	IN0 Reading
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R
Mode 1								
Definition	IN7 Reading	IN6 Reading	IN5 Reading	IN4 Reading	IN3 Reading	IN2 Reading	IN1 Reading	IN0 Reading
Default Value	0	0	0	0	0	0	0	0
Attribution	R	R	R	R	R	R	R	R

Address	Name	Description
Mode 0		
0x20	IN0 Reading	Reading for this perspective channel
0x21	IN1 Reading	Reading for this perspective channel
0x22	IN2 Reading	Reading for this perspective channel
0x23	IN3 Reading	Reading for this perspective channel
0x24	IN4 Reading	Reading for this perspective channel
0x25	IN5 Reading	Reading for this perspective channel
0x26	IN6 Reading	Reading for this perspective channel
0x27	Temperature Reading	Reading for this perspective channel
Mode 1		
0x20	IN0 Reading	Reading for this perspective channel
0x21	IN1 Reading	Reading for this perspective channel
0x22	IN2 Reading	Reading for this perspective channel
0x23	IN3 Reading	Reading for this perspective channel
0x24	IN4 Reading	Reading for this perspective channel
0x25	IN5 Reading	Reading for this perspective channel
0x26	IN6 Reading	Reading for this perspective channel
0x27	IN7 Reading	Reading for this perspective channel

The channel conversion readings are available in registers 20h to 27h. Each register is 16-bit wide to accommodate the 12-bit voltage reading or 12-bit temperature reading. Conversions can be read at any time and will provide the result of the last conversion. If a conversion is in progress while a communication is started, that conversion will be completed, and the Channel Reading Registers will not be updated until the communication is complete.

Limit Registers - Addresses - 0x2A - 0x39

Table 14 Address 0x2A – 0x39

Register Address	0x31	0x30	0x2F	0x2E	0x2D	0x2C	0x2B	0x2A
Mode 0								
Definition	IN3 Low Limit	IN3 High Limit	IN2 Low Limit	IN2 High Limit	IN1 Low Limit	IN1 High Limit	IN0 Low Limit	IN0 High Limit
Default Value	0x00	0xFF	0x00	0xFF	0x00	0xFF	0x00	0xFF
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 1								
Definition	IN3 Low Limit	IN3 High Limit	IN2 Low Limit	IN2 High Limit	IN1 Low Limit	IN1 High Limit	IN0 Low Limit	IN0 High Limit
Default Value	0x00	0xFF	0x00	0xFF	0x00	0xFF	0x00	0xFF
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Limit Registers - Addresses - 0x2A - 0x39(continued)

Register Address	0x39	0x38	0x37	0x36	0x35	0x34	0x33	0x32
Mode 0								
Definition	Temperature Hysteresis Limit	Temperature High Limit	IN6 Low Limit	IN6 High Limit	IN5 Low Limit	IN5 High Limit	IN4 Low Limit	IN4 High Limit
Default Value	0x45	0x55	0x00	0xFF	0x00	0xFF	0x00	0xFF
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 1								
Definition	IN7 Low Limit	IN7 High Limit	IN6 Low Limit	IN6 High Limit	IN5 Low Limit	IN5 High Limit	IN4 Low Limit	IN4 High Limit
Default Value	0x45	0x55	0x00	0xFF	0x00	0xFF	0x00	0xFF
Attribution	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Limit Registers - Addresses - 0x2A - 0x39(continued)

`	Name	Description
Mode 0		
0x2A	IN0 High Limit	High Limit
0x2B	IN0 Low Limit	Low Limit
0x2C	IN1 High Limit	High Limit
0x2D	IN1 Low Limit	Low Limit
0x2E	IN2 High Limit	High Limit
0x2F	IN2 Low Limit	Low Limit
0x30	IN3 High Limit	High Limit
0x31	IN3 Low Limit	Low Limit
0x32	IN4 High Limit	High Limit

0x33	IN4 Low Limit	Low Limit
0x34	IN5 High Limit	High Limit
0x35	IN5 Low Limit	Low Limit
0x36	IN6 High Limit	High Limit
0x37	IN6 Low Limit	Low Limit
0x38	Temperature High Limit	High Limit
0x39	Temperature Hysteresis Limit	Hysteresis Limit

Limit Registers - Addresses - 0x2A - 0x39(continued)

`	Name	Description
Mode1		
0x2A	IN0 High Limit	High Limit
0x2B	IN0 Low Limit	Low Limit
0x2C	IN1 High Limit	High Limit
0x2D	IN1 Low Limit	Low Limit
0x2E	IN2 High Limit	High Limit
0x2F	IN2 Low Limit	Low Limit
0x30	IN3 High Limit	High Limit
0x31	IN3 Low Limit	Low Limit
0x32	IN4 High Limit	High Limit
0x33	IN4 Low Limit	Low Limit
0x34	IN5 High Limit	High Limit
0x35	IN5 Low Limit	Low Limit
0x36	IN6 High Limit	High Limit
0x37	IN6 Low Limit	Low Limit
0x38	IN7 High Limit	High Limit
0x39	IN7 Low Limit	Low Limit

Manufacturer ID Register - 0x3E

Table 15 address 0x3E

Register Address 0x3E	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Manufacturer ID							
Default Value	0x59							
Attribution	R							

Revision ID Register - 0x3F

Table 16 Address 0x3F

Register Address 0x3F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Definition	Revision ID							
Default Value	0x21							
Attribution	R							

Application and Implementation

Digital Output (D_{OUT})

The digital output code for a 12-bit ADC can be calculated as:

$D_{OUT} = [\Delta VIN / V_{REF}] \times 2^{12}$

For equation, ΔVIN = INx – GND, where 0 ≤ x ≤ 7, for the single-ended configuration. In theory, ΔVIN can be of any value between 0 V and (V_{REF}-LSb). Any ΔVIN value outside of this range will produce a digital output code of 0 or 4095.

Temperature Measurement System

The local temperature measurement data is in the local temperature register (read only attribution, Reg Add, 0x27h). For 12 bit format, the temperature data is composed by 2 bytes, MSB plus LSB, which can be get in same time using I²C 2 bytes reading. The 1st byte is eight most significant bits [MSB] plus least significant bits [LSB].The data range is from 0x000 to 0x7FF, which means the expressed temperature range is from -128ºC to 127.9375ºC with 0.0625ºC LSB. Note that 2 bytes is a signed bit value.

Table 17 Temperature Registers Sample Temperatures

Measured Temperature (ºC)	Digital Output (HEX, high 12bit effect)	Digital Output (DEC, in signed number)	Digital Output (BIN) (MSB)	Digital Output (BIN) (LSB)
+127.9375	0x7FF0	32752	0 1 1 1 ,1 1 1 1	1 1 1 1 ,0 0 0 0
+125	0x7D00	32000	0 1 1 1, 1 1 0 1	0 0 0 0 ,0 0 0 0
+25	0x1900	6400	0 0 0 1, 1 0 0 1	0 0 0 0 ,0 0 0 0
+0.0625	0x0010	16	0 0 0 0, 0 0 0 0	0 0 0 1 ,0 0 0 0
0.0	0x0000	0	0 0 0 0, 0 0 0 0	0 0 0 0 ,0 0 0 0
-0.0625	0xFFF0	-16	1 1 1 1, 1 1 1 1	1 1 1 1 ,0 0 0 0
-25	0xE700	-6400	1 1 1 0, 0 1 1 1	0 0 0 0 ,0 0 0 0
-40	0xD800	-10240	1 1 0 1, 1 0 0 0	0 0 0 0 ,0 0 0 0

In general, the easiest way to calculate the temperature (℃) is to use the following formulas:

For 12 bit: $T = \frac{R_{value\ \&\ 0xFFF0}}{256}$ （ºC）

Where the R_{value} is the two bytes data of Reg. 0x27 and the T is the temperature data in signed number format. “&” is the bitwise AND operation.”& 0xFFF0” means the effect value is the high 12bits. For example, if Reg. 0x27 is 0xE878, (0xE878 & 0xFFF0) = 0xE870 = -6032 in decimal, so the temperature is -6032/256=-23.5625 ºC.

Temperature Limits

One of the PJ79818 features is monitoring the temperature reading. This monitoring is accomplished by setting a temperature limit to the Temperature High Limit Register (T_{hot}, address 0x38) and Temperature Hysteresis Limit Register (T_{hot_hyst}, address 0x39). When the temperature reading ≥ T_{hot}, an interrupt occurs. How this interrupt occurs will be explained in Temperature Interrupt.

Each temperature limit is represented by an 8-bit, two's complement word with a least significant bit (LSb) equal to 1°C. Table 19 shows some sample temperatures that can be programmed to the Temperature Limit Registers. In general, use the following equations to calculate the digital code that represents the desired temperature limit:

If Temp Limit (°C) ≥ 0: Digital Code (dec) = Temp Limit(°C)

If Temp Limit (°C) < 0: Digital Code (dec) = 2^8 – |Temp Limit(°C)|

Table 18 Temperature Limit Registers Sample Temperatures

TEMP LIMIT	DIGITAL OUTPUT (D_{OUT})		
	BINARY [MSb...LSb]	DECIMAL	HEX
+125°C	0111_1101	125	7D
+25°C	0001_1001	25	19
+1.0°C	0000_0001	1	01
+ 0°C	0000_0000	0	00
-1.0°C	1111_1111	255	FF
-25°C	1110_1111	231	E7
-40°C	1101_1000	216	D8

Interrupt Structure

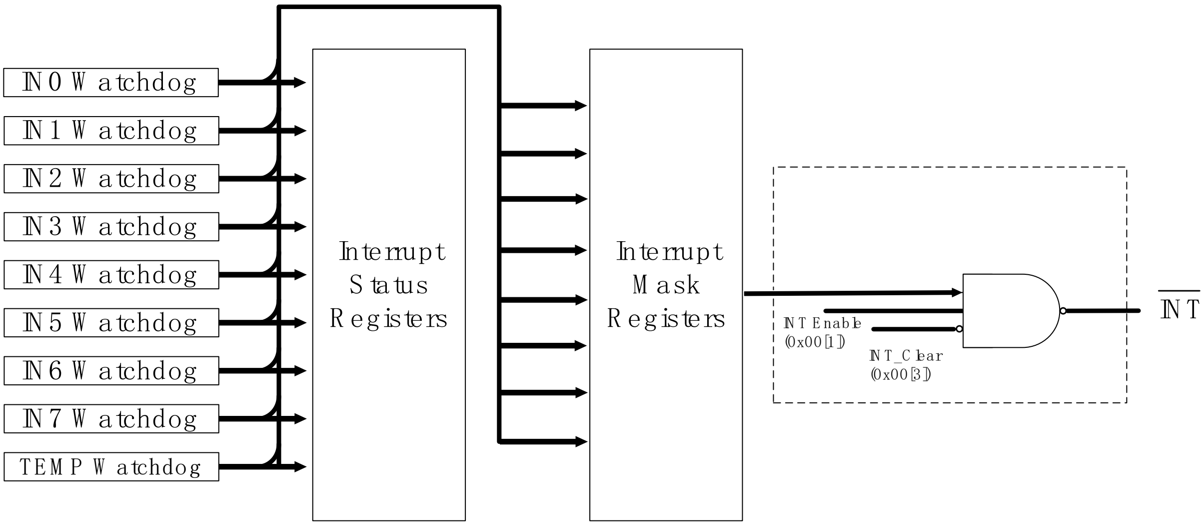


Figure 11 Interrupt Structure

Interrupt Output ($\overline{INT}$)

PJ79818 generates an interrupt as a result of each of its internal WATCHDOG registers on the voltage and temperature channels. In general, $\overline{INT}$ becomes active when all three scenarios, as depicted in Figure 11 occur:

1. '$\overline{INT}$_Clear' (0x00 [3]) = 0.
2. '$\overline{INT}$_Enable' (0x00 [1]) = 1 to enable interrupt output.
3. The voltage reading ≥ the voltage high limit or < the voltage low limit, or the temperature reading ≥ T_{hot} limit.

Interrupt Clearing

There are four methods to clear interrupts.

1. Reading the Interrupt Status Register (addresses 0x01) will output the contents of the register and clear the register. When the Interrupt Status Register clears, the $\overline{\text{INT}}$ pin also clears until this register is updated by the round-robin monitoring loop.
2. Set $\overline{\text{INT}}$_Clear bit (address 0x00, bit 3) = 1. When this bit is high, the $\overline{\text{INT}}$ pin and Interrupt Status Register will clears at the same time.
3. When the voltage interrupt event occurs, the voltage reading falls down the voltage high limit or above the voltage low limit (the voltage low limit ≤ the voltage reading < the voltage high limit), the $\overline{\text{INT}}$ pin and Interrupt Status Register will be cleared automatically. Similarly, when temperature triggers an interrupt, if the temperature reading falls down the hysteresis value (the temperature reading ≤ the hysteresis limit < the temperature high limit), the $\overline{\text{INT}}$ pin and Interrupt Status Register will be cleared automatically too.
4. The channel corresponding to the trigger interrupt is set to interrupt masking, the $\overline{\text{INT}}$ pin will be cleared, but the interrupt status bit corresponding to the trigger interrupt isn't cleared.

Temperature Interrupt

One of the PJ79818 features is monitoring the temperature reading. This monitoring is accomplished by setting a temperature limit to the Temperature High Limit Register (T_{hot}, address 0x38) and Temperature Hysteresis Limit Register (T_{hot_hyst}, address 0x39). These limit registers have an interrupt mode, shown in Figure 11 that operates in the following way: if the temperature reading ≥ T_{hot}, an interrupt will occur and will remain active indefinitely until reset by reading the Interrupt Status Register (address 0x01).

Once an interrupt event has occurred by crossing T_{hot}, then reset, an interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature reading is < T_{hot_hyst} or a read of the Interrupt Status Register has occurred when the temperature falls down T_{hot}.

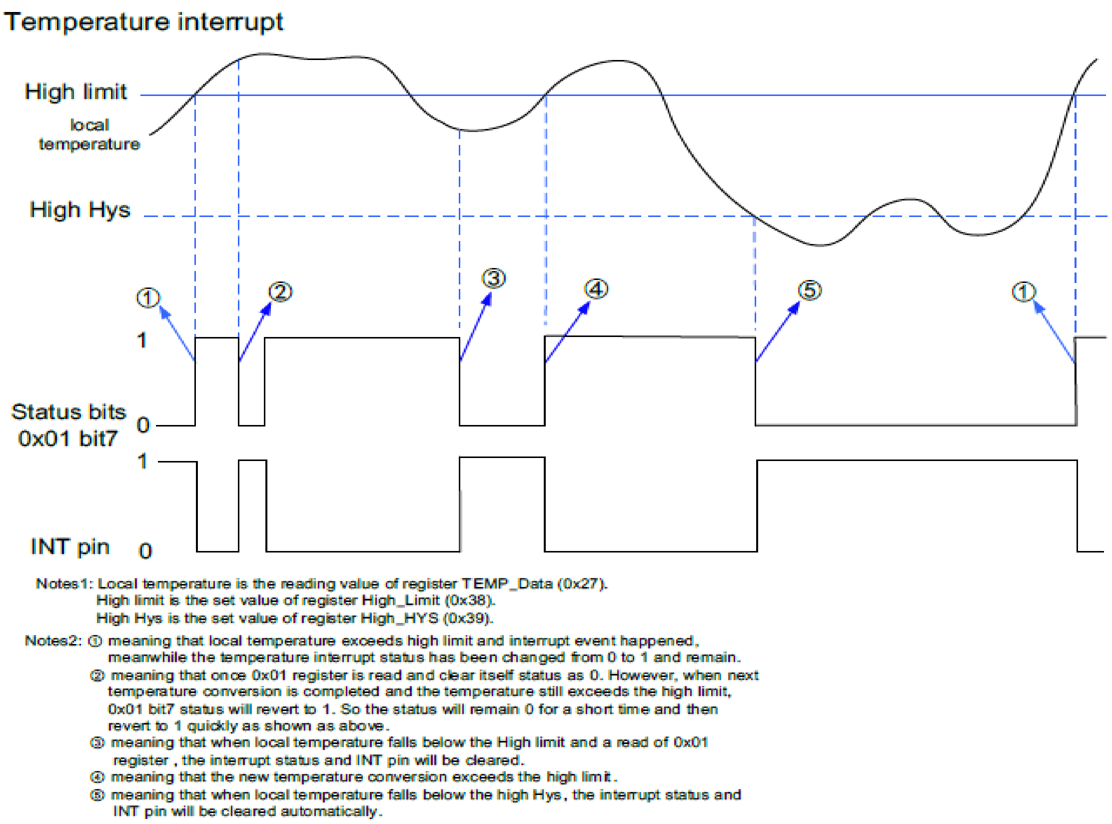


Figure 12 Temperature Response Structure

Design Requirements

In this typical hardware monitor application, several different sources are being monitored by the PJ79818. First, an external temperature sensor is being monitored. An external temperature sensor is frequently used to monitor ambient temperature of the system.

Detailed Design Procedure

To understand the average supply current (I_{CC}), the conversion rates must be introduced. PJ79818 has three types of conversion rates: Continuous Conversion Mode, Low Power Conversion Mode, and One Shot Mode. In the Low Power Conversion Mode, the device converts all of the enabled channels then enters shutdown mode; this process takes approximately 874ms to complete. (More information on the conversion rate will be discussed in the Conversion Rate Register - Address 0x07 and One-Shot Register - Address 0x09 sections).

Each type of conversion produces a different average supply current. The supply current for a voltage conversion will be referred to as I_{CC_VOL}, a temperature conversion as I_{CC_TEMP}, and the shutdown mode as $I_{CC\_SHUTDOWN}$. These values can be obtained from Typical Performance Characteristics plots.

In general, I_{CC} is the average supply current while PJ79818 is operating in the Low Power Conversion Mode with all of the available channels enabled. Its plot can be seen in Typical Characteristics and its equation,

$$I_{CC} = [(0.015)(b)(I_{CC\_VOL})] + [(0.002)(a)(I_{CC\_TEMP})] + [1 - (0.002)(a) - 0.015(b)](I_{CC\_SHUTDOWN})]$$

where

- a is the number of local temperature available.
- b is the number of ENABLED voltage channel.

Each mode of operation has a different "a" and "b" values. The following table shows the value for "a" and the maximum value for "b" for each mode.

Table 19 "a" and "b" Values

	a	b(MAX)
Mode 0	1	7
Mode 1	0	8

Quick Start

1. Power on the device, and then wait for at least 33ms.
2. Read the Busy Status Register (address 0x0C). If the 'Not Ready' bit = 1, then increase the wait time until 'Not Ready' bit = 0 before proceeding to the next step.
3. Program the Advanced Configuration Register - Address 0x0B:
   - a. Choose to use the internal or external V_{REF} (bit 0).
   - b. Choose the mode of operation (bits 1).
4. Program the Conversion Rate Register (address 0x07).
5. Choose to enable or disable the channels using the Channel Disable Register (address 0x08).
6. Using the Interrupt Mask Register (address 0x03), choose to mask or not to mask the interrupt status from propagating to the interrupt output pin ($\overline{\text{INT}}$).
7. Program the Limit Registers (addresses 0x2A - 0x39).
8. Set the 'START' bit of the Configuration Register (address 0x00h, bit 0) to 1.
9. Set the '$\overline{\text{INT}}$_Clear' bit (address 0x00, bit 3) to 0. If needed, program the "$\overline{\text{INT}}$_Enable" bit (address 0x00, bit 1) to 1 to enable the $\overline{\text{INT}}$ output.

The PJ79818 then performs a round-robin monitoring of enabled voltage and temperature channels. The sequence of items being monitored corresponds to locations in the Channel Readings Registers (except for the temperature reading). Detailed descriptions of the register map can be found at the end of this data sheet.

Power on Reset (POR)

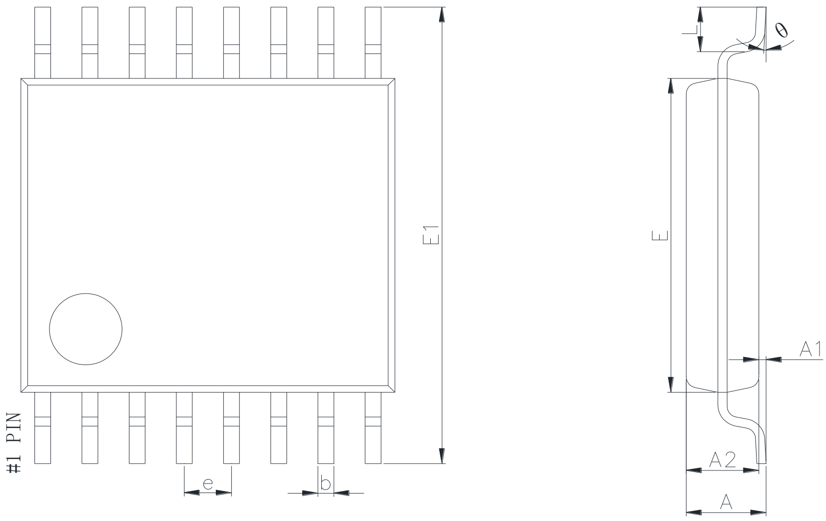
When power is first applied, the PJ79818 performs a power on reset (POR) on several of its registers, which sets the registers to their default values. These default values are shown in Table 4 or in Register Maps. Registers whose default values are not shown have power on conditions that are indeterminate.

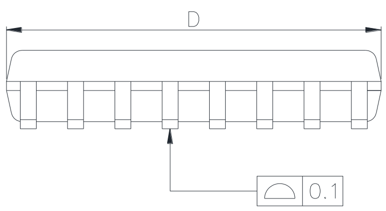
Package Outline Dimensions and Recommend Land Pattern Layout

TSSOP-16P

Package Outline Dimensions

TSSOP-16P Unit (mm)

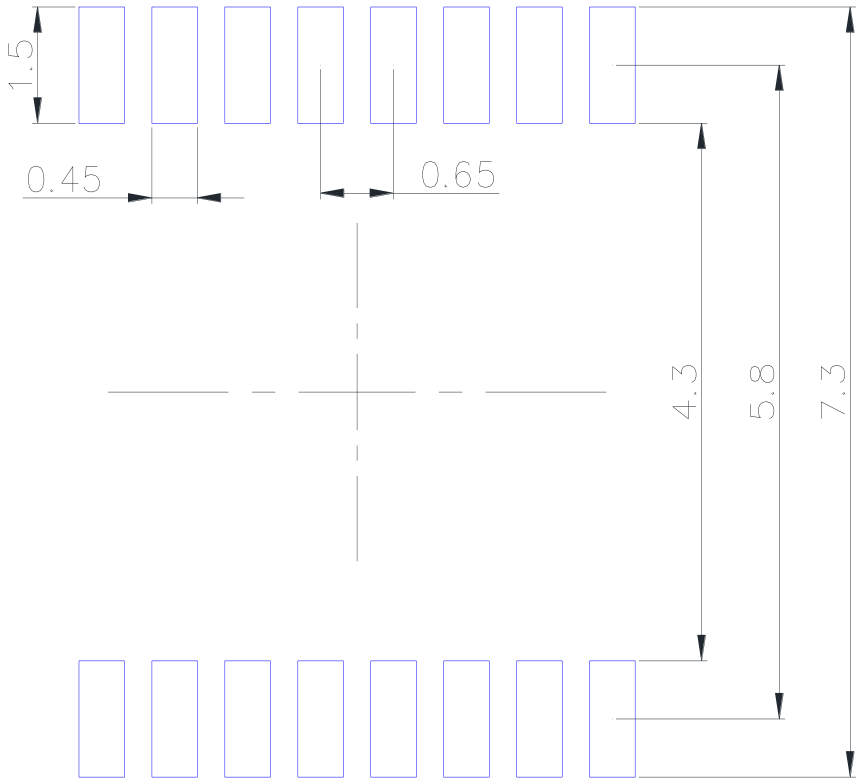




Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650（BSC）		0.026（BSC）	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommended Land Pattern Layout

TSSOP-16P Unit (mm)



Note:

1 All dimensions are in millimeter

2 Recommend tolerance is within ±0.1mm

3 Change without notice

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