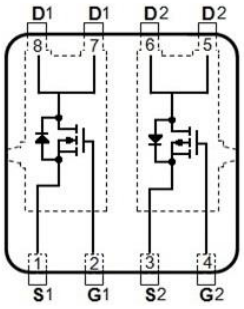
PJQ4670AP

100V Complementary Enhancement Mode MOSFET

Voltage	100/-100 V	Current	10 / -7 A

DFN3333B-8L



Features

- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 Standard

Mechanical Data

- Case: DFN3333B-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0271 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	N-CH LIMIT	P-CH LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	-100	V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current(Note 4)	T_C=25°C	I_D	10	-7	A
	T_C=100°C		6.5	-4.4	
Pulsed Drain Current(Note 1)	T_C=25°C	I_{DM}	17	-10	
Power Dissipation	T_C=25°C	P_D	30		W
	T_C=100°C		12		
Continuous Drain Current(Note 4)	T_A=25°C	I_D	2.7	-1.8	A
	T_A=70°C		2.1	-1.4	
Power Dissipation	T_A=25°C	P_D	1.9		W
	T_A=70°C		1.2		
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150		°C
Single Pulse Avalanche Current(Note 5,6)		I_{AS}	2.9	-3.6	A
Single Pulse Avalanche Energy(Note 5,6)		E_{AS}	3.9	6.1	mJ
Typical Thermal Resistance(Note 4)	Junction to Case	$R_{\theta JC}$	4.1		°C/W
	Junction to Ambient	$R_{\theta JA}$	65		

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N-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1	1.6	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A	-	98	118	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=1A	-	102	128	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=50V, I_D=2A, V_{GS}=10V(Note 2,3)	-	17.8	24	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	2.7	-	
Input Capacitance	Ciss	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	863	1210	pF
Output Capacitance	Coss		-	29	51	
Reverse Transfer Capacitance	Crss		-	17	30	
Gate resistance	R_g	f=1MHz	-	2	-	Ω
Turn-On Delay Time	$td_{(on)}$	V_{DS}=50V, I_D=2A, V_{GS}=10V, R_G=3Ω (Note 2,3)	-	5.6	-	ns
Turn-On Rise Time	t_r		-	2.6	-	
Turn-Off Delay Time	$td_{(off)}$		-	21	-	
Turn-Off Fall Time	t_f		-	2.4	-	
Drain-Source Diode						
Diode Forward Current	I_S	T_C=25°C	-	-	10	A
Pulsed Diode Forward Current	I_{SM}		-	-	17	
Diode Forward Voltage	V_{SD}	I_S=2A, V_{GS}=0V	-	0.8	1.3	V
Reverse Recovery Time	Trr	V_{DD}=50V,V_{GS}=0V	-	28	-	ns
Reverse Recovery Charge	Qrr	I_S=10A,dI_S/dt=100A/us	-	14	-	nC

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P-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250uA	-100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-1	-1.8	-2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-2A	-	246	295	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-1A	-	263	329	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=-50V, I_D=-2A V_{GS}=-10V(Note 1,2)	-	19.7	26	nC
Gate-Source Charge	Q_{gs}		-	3.4	-	
Gate-Drain Charge	Q_{gd}		-	3	-	
Input Capacitance	Ciss	V_{DS}=-50V, V_{GS}=0V f=1MHZ	-	885	1240	pF
Output Capacitance	Coss		-	31	55	
Reverse Transfer Capacitance	Crss		-	21	37	
Gate resistance	R_g	f=1MHz	-	15	-	Ω
Turn-On Delay Time	$td_{(on)}$	V_{DS}=-50V, I_D=-2A V_{GS}=-10V, R_G=3Ω (Note 1,2)	-	5.8	-	ns
Turn-On Rise Time	t_r		-	3.5	-	
Turn-Off Delay Time	$td_{(off)}$		-	44	-	
Turn-Off Fall Time	t_f		-	16	-	
Drain-Source Diode						
Diode Forward Current	I_S	T_C=25°C	-	-	-7	A
Pulsed Diode Forward Current	I_{SM}		-	-	-10	
Diode Forward Voltage	V_{SD}	I_S=-2A, V_{GS}=0V	-	-0.85	-1.3	V
Reverse Recovery Time	Trr	V_{DD}=-50V,V_{GS}=0V	-	25	-	ns
Reverse Recovery Charge	Qrr	I_S=-7A,dI_S/dt=100A/us	-	27	-	nC

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. E_{AS} of N-CH is calculated based on the condition of L=1mH, I_{AS}=2.8A, V_{DD}=30V, V_{GS}=10V. 100% test at L=0.5mH, I_{AS}=2.9A in production.
6. E_{AS} of P-CH is calculated based on the condition of L=1mH, I_{AS}=-3.5A, V_{DD}=-30V, V_{GS}=-10V. 100% test at L=0.5mH, I_{AS}=-3.6A in production.
7. Guaranteed by design, not subject to production testing.

PJQ4670AP

N-CH TYPICAL CHARACTERISTIC CURVES

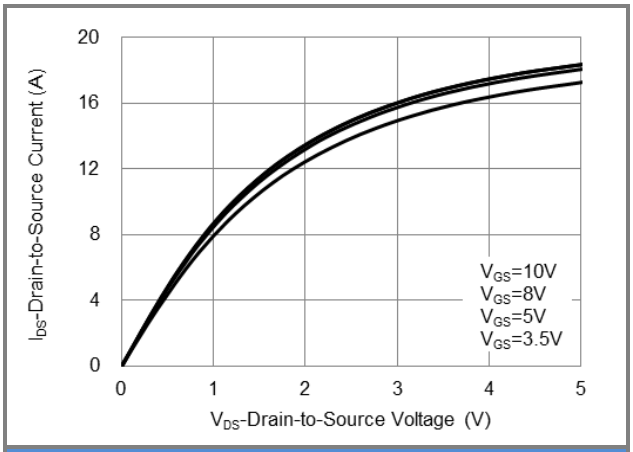

Fig.1 Output Characteristics

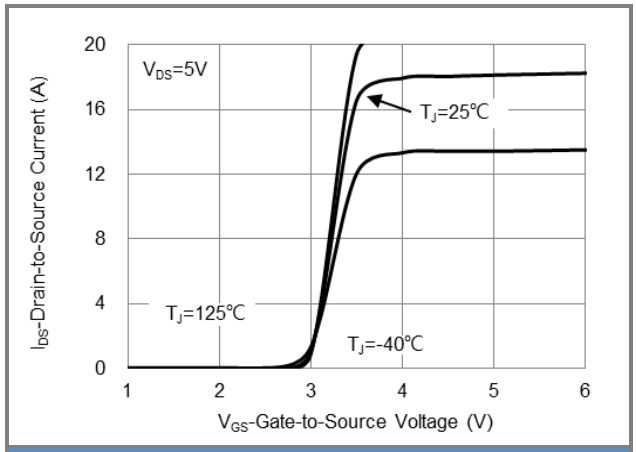

Fig.2 Transfer Characteristics

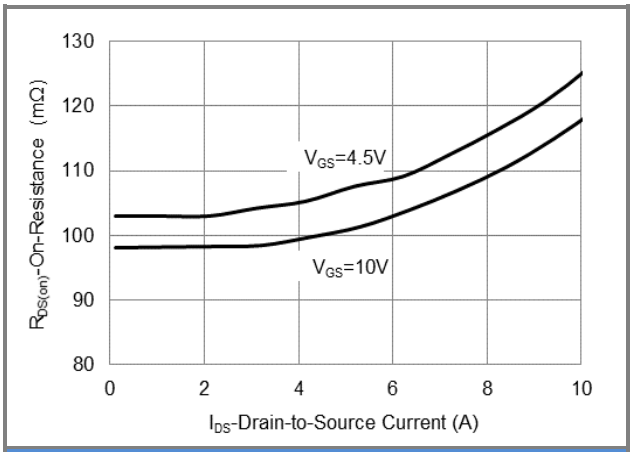

Fig.3 On-Resistance vs. Drain Current

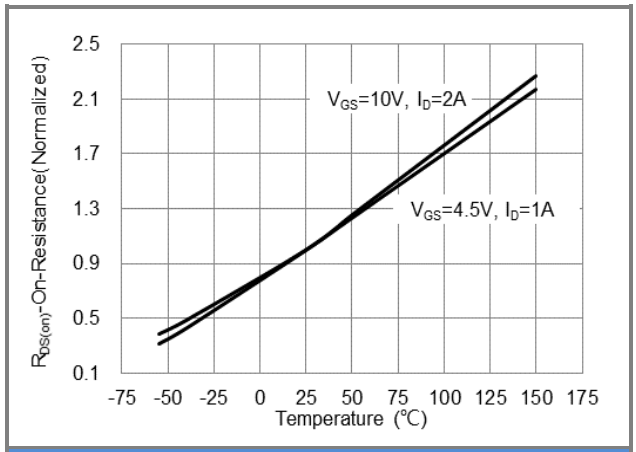

Fig.4 On-Resistance vs. Junction temperature

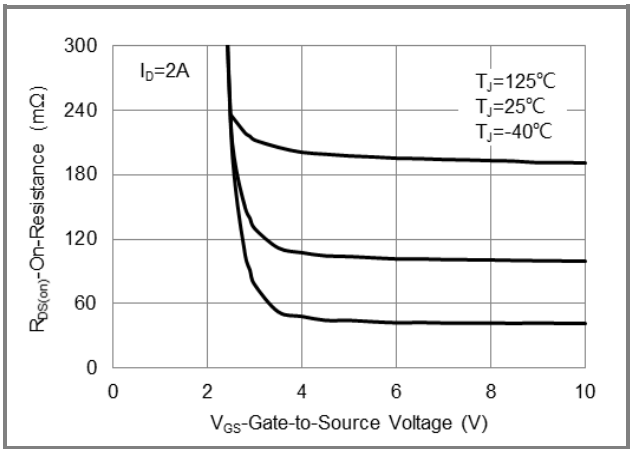

Fig.5 On-Resistance Variation with V_{GS}

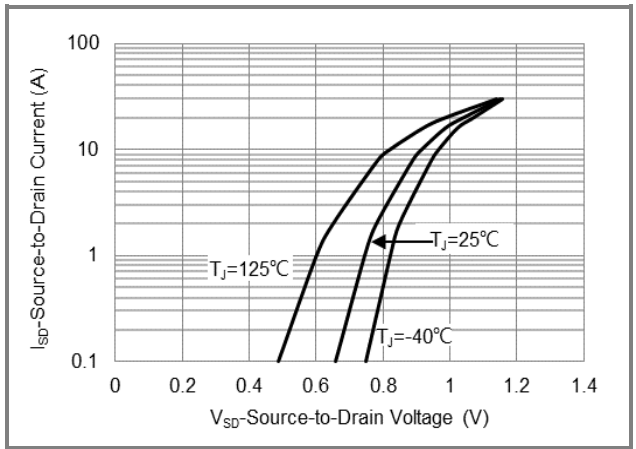

Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

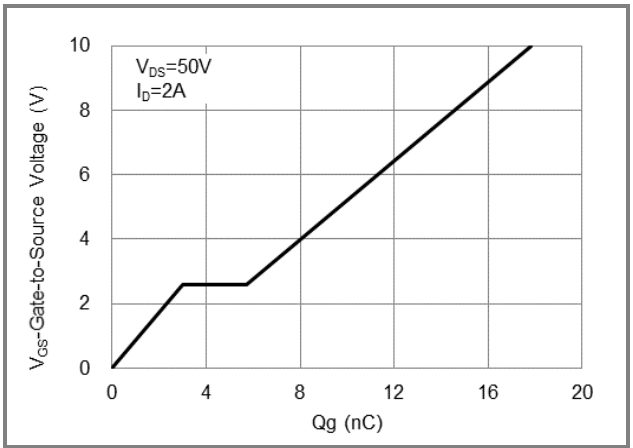

Fig.7 Gate-Charge Characteristics

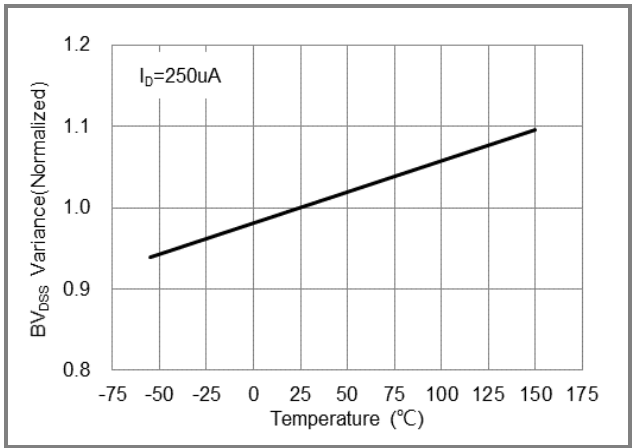

Fig.8 Breakdown Voltage Variation vs. Temperature

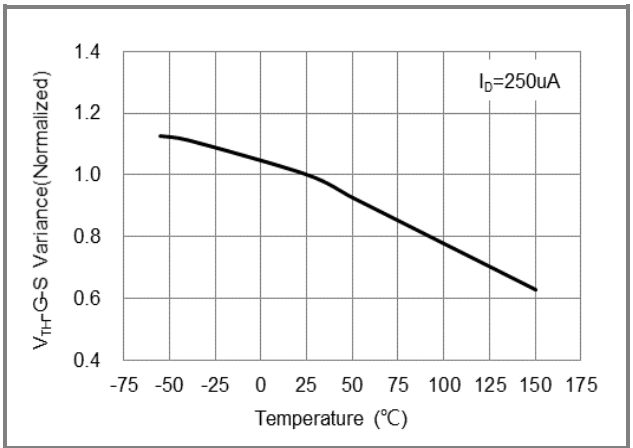

Fig.9 Threshold Voltage Variation with Temperature

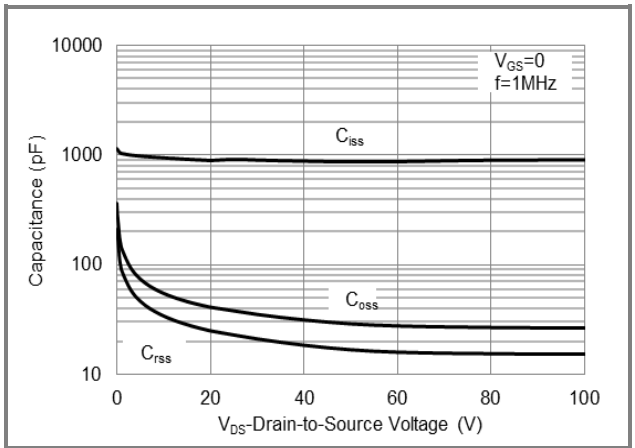

Fig.10 Capacitance vs. Drain-Source Voltage

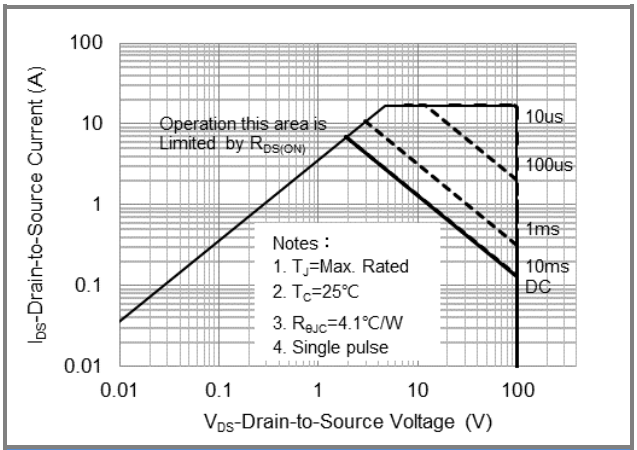

Fig.11 Maximum Safe Operating Area

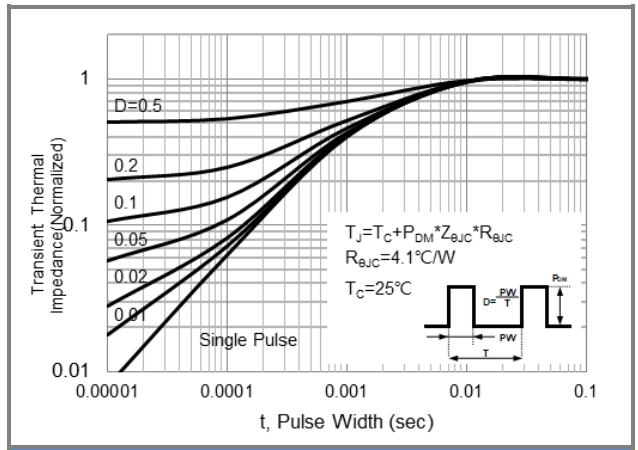

Fig.12 Normalized Transient Thermal Impedance

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P-CH TYPICAL CHARACTERISTIC CURVES

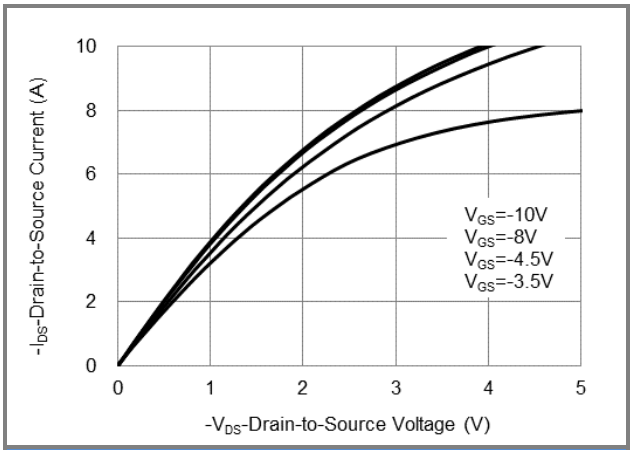


Fig.13 Output Characteristics

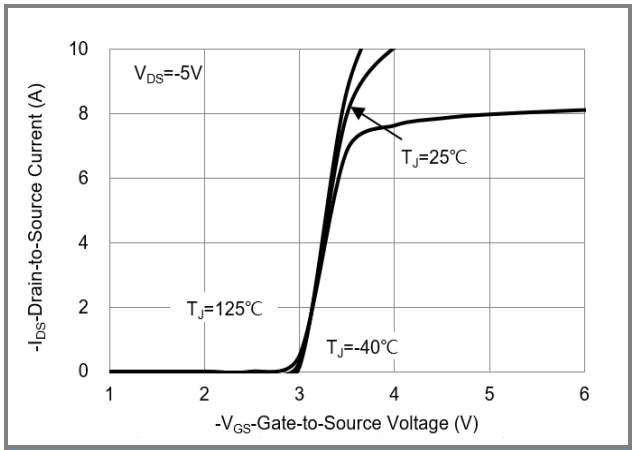


Fig.14 Transfer Characteristics

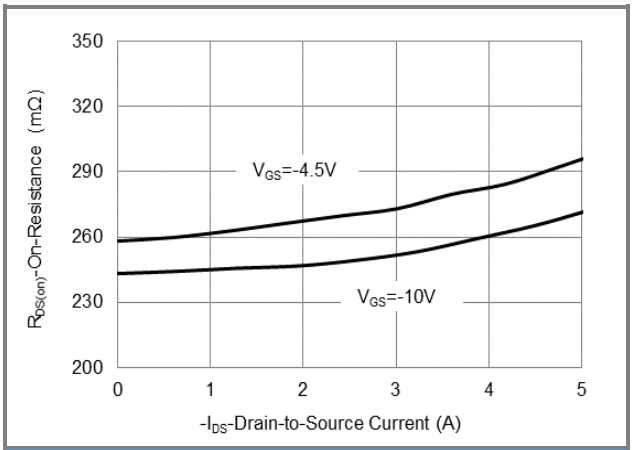


Fig.15 On-Resistance vs. Drain Current

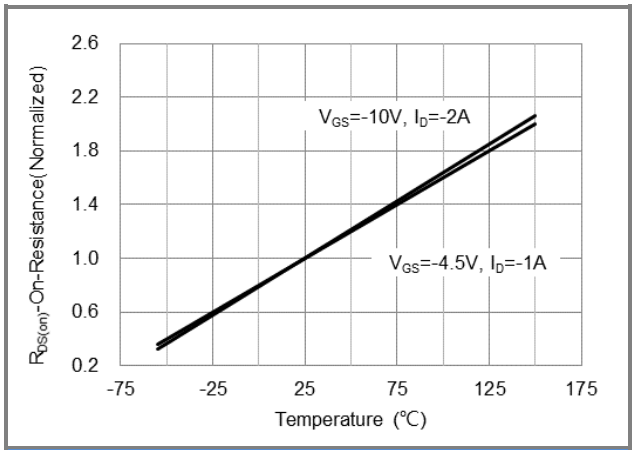


Fig.16 On-Resistance vs. Junction temperature

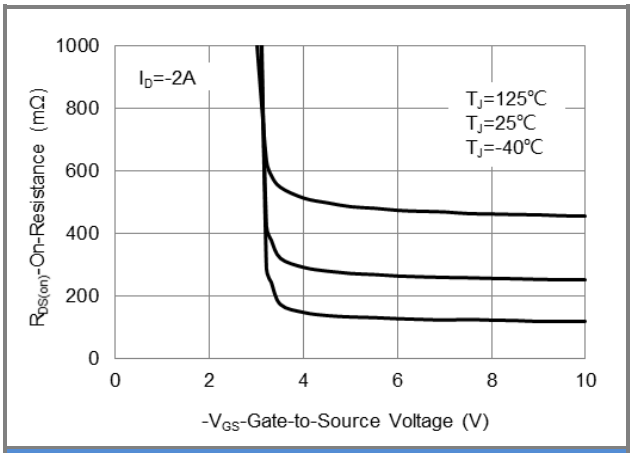


Fig.17 On-Resistance Variation with V_{GS}

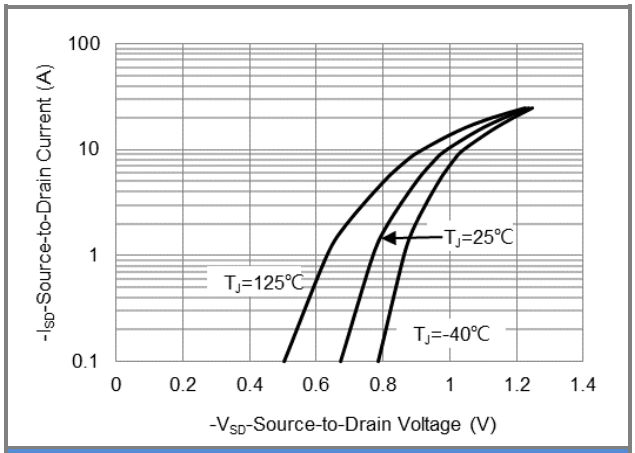


Fig.18 Source-Drain Diode Forward Voltage

PJQ4670AP

TYPICAL CHARACTERISTIC CURVES

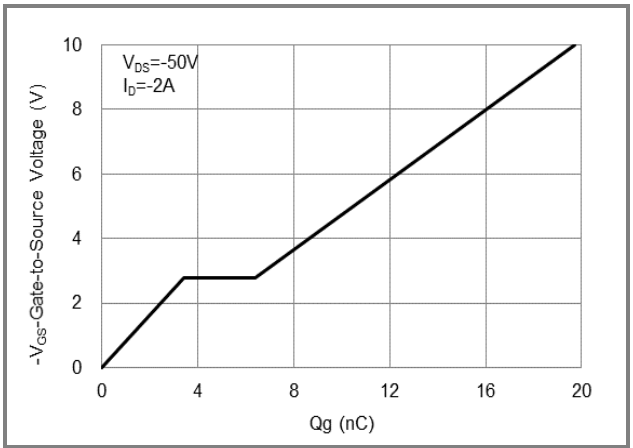


Fig.19 Gate-Charge Characteristics

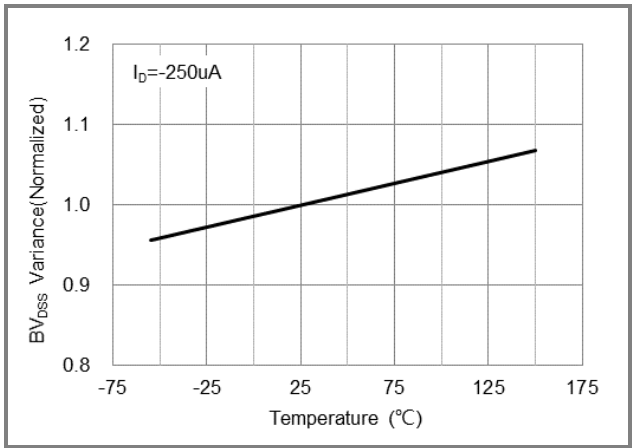


Fig.20 Breakdown Voltage Variation vs. Temperature

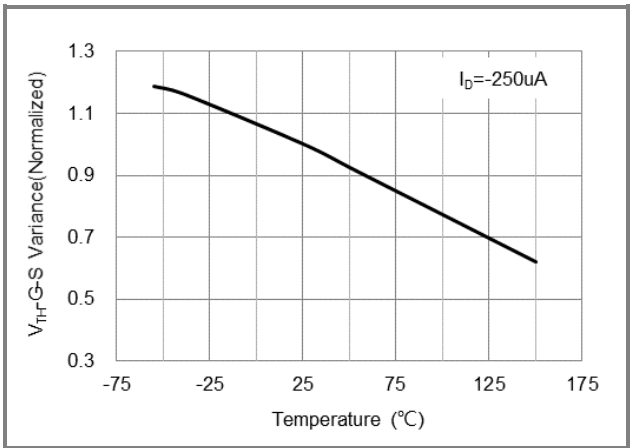


Fig.21 Threshold Voltage Variation with Temperature

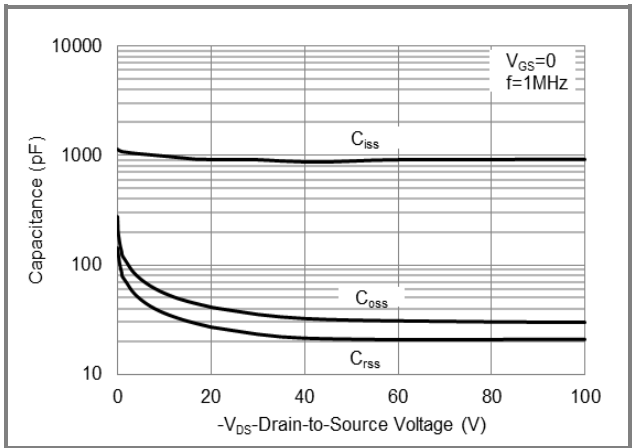


Fig.22 Capacitance vs. Drain-Source Voltage

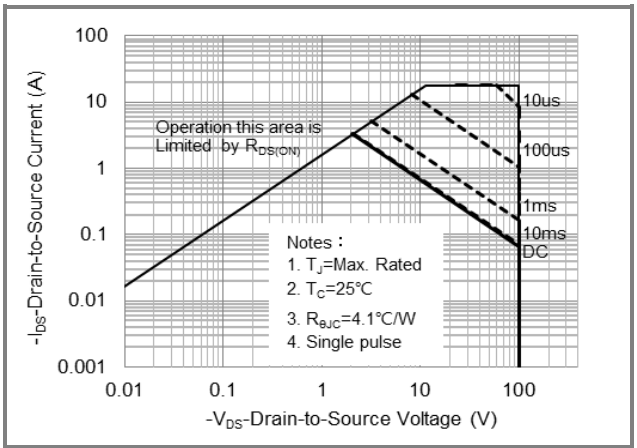


Fig.23 Maximum Safe Operating Area

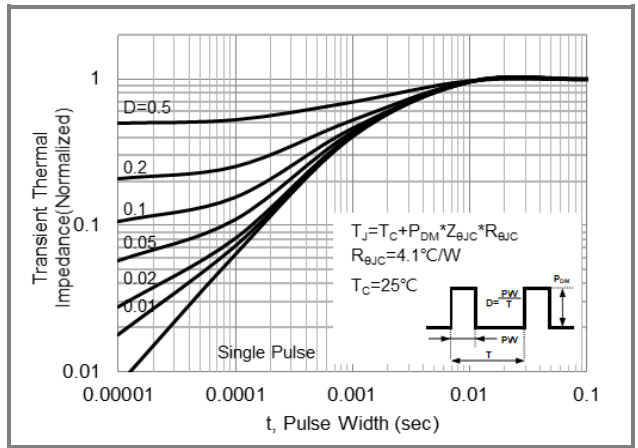


Fig.24 Normalized Transient Thermal Impedance

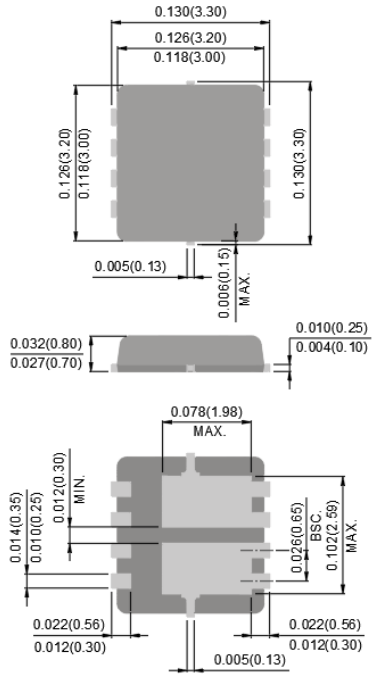
PJQ4670AP

Product and Packing Information

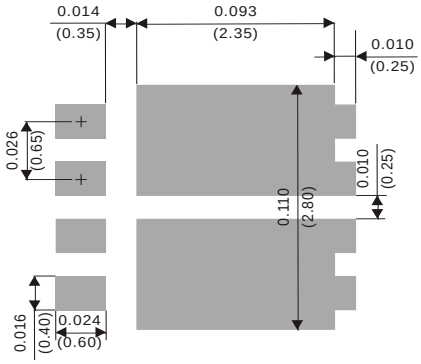
Part No.	Package Type	Packing Type	Marking
PJQ4670AP	DFN3333B-8L	5K pcs / 13” reel	670A

Packaging Information & Mounting Pad Layout

DFN3333B-8L Dimension — Unit: inch(mm)



DFN3333B-8L Pad Layout — Unit: inch(mm)



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