

PJQ4544S6P-AU

40V N-Channel Enhancement Mode MOSFET

Voltage **40 V** **Current** **100 A**

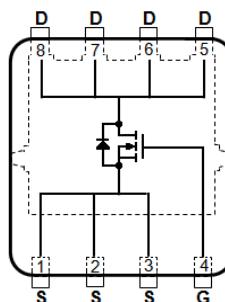
Features

- $R_{DS(ON)}$, $V_{GS} @ 10V$, $I_D @ 20A < 3.6m\Omega$
- $R_{DS(ON)}$, $V_{GS} @ 4.5V$, $I_D @ 10A < 5.7m\Omega$
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	I_D	100	A
$T_C=100^\circ C$		72	
Pulsed Drain Current ^(Note 1)	I_{DM}	400	W
Power Dissipation	P_D	65	
$T_C=100^\circ C$		33	
Continuous Drain Current ^(Note 4)	I_D	20	A
$T_A=70^\circ C$		16.7	
Power Dissipation	P_D	2.5	W
$T_A=70^\circ C$		1.8	
Single Pulse Avalanche Current ^(Note 5)	I_{AS}	12.6	A
Single Pulse Avalanche Energy ^(Note 5)	E_{AS}	71	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~175	°C
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	°C/W
	Junction to Ambient	$R_{\theta JA}$	

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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	40	-	-	V
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	1.2	1.6	2.2	
Drain-Source On-State Resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=20\text{A}$	-	2.9	3.6	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=10\text{A}$	-	4.4	5.7	
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=40\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	±100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=32\text{V}, \text{I}_D=20\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$ ^(Note 2)	-	43	56	nC
Gate-Source Charge	Q_{gs}		-	5.7	-	
Gate-Drain Charge	Q_{gd}		-	7.2	-	
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $f=1\text{MHz}$	-	1405	1830	pF
Output Capacitance	C_{oss}		-	440	660	
Reverse Transfer Capacitance	Crss		-	45	80	
Gate resistance	R_g	$f=1\text{MHz}$	-	1.8	-	Ω
Turn-On Delay Time	$\text{t}_{\text{d(on)}}$	$\text{V}_{\text{DS}}=32\text{V}, \text{I}_D=20\text{A},$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_g=3\Omega$ ^(Note 2)	-	7.1	-	ns
Turn-On Rise Time	t_r		-	10.5	-	
Turn-Off Delay Time	$\text{t}_{\text{d(off)}}$		-	32	-	
Turn-Off Fall Time	t_f		-	14	-	
Drain-Source Diode						
Diode Forward Current	I_s	$\text{T}_c=25^\circ\text{C}$ (Package Limit)	-	-	70	A
Pulsed Diode Forward Current	I_{SM}		-	-	400	
Diode Forward Voltage	V_{SD}	$\text{I}_s=20\text{A}, \text{V}_{\text{GS}}=0\text{V}$	-	0.8	1.3	V
Reverse Recovery Time	Tr_{r}	$\text{V}_{\text{DD}}=32\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $\text{I}_s=20\text{A}, \text{dI}_{\text{S}}/\text{dt}=100\text{A}/\text{us}$ ^(Note 2)	-	34	-	ns
Reverse Recovery Charge	Q_{rr}		-	16	-	

NOTES :

1. Pulse width $\leq100\mu\text{s}$, Duty cycle $\leq2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an $R_{\text{EJC}}=2.3^\circ\text{C}/\text{W}$.
4. R_{EJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of $L=1\text{mH}, I_{\text{AS}}=11.9\text{A}, V_{\text{DD}}=30\text{V}, V_{\text{GS}}=10\text{V}$. 100% test at $L=0.5\text{mH}, I_{\text{AS}}=12.6\text{A}$ in production.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

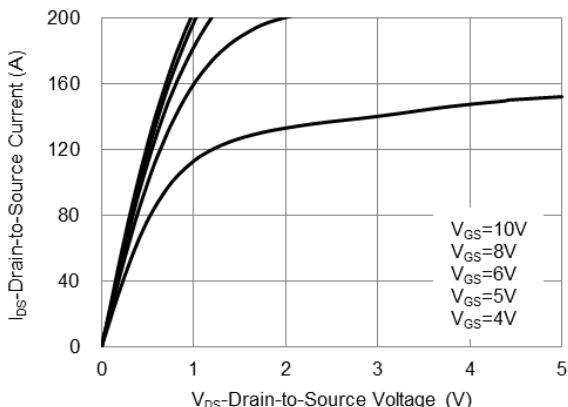


Fig.1 On-Region Characteristics

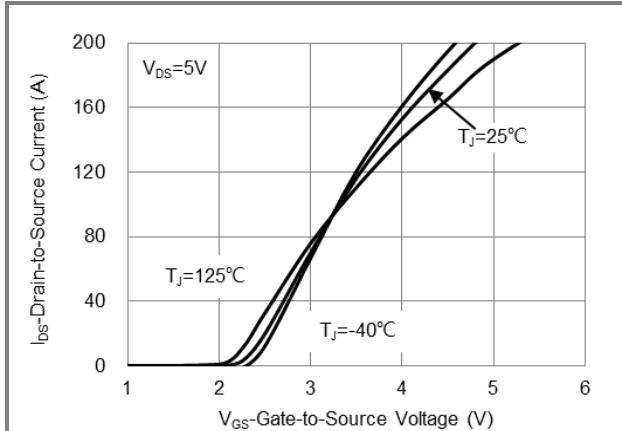


Fig.2 Transfer Characteristics

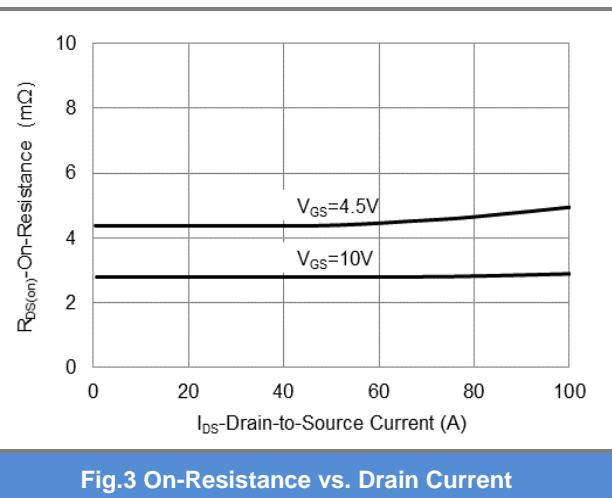


Fig.3 On-Resistance vs. Drain Current

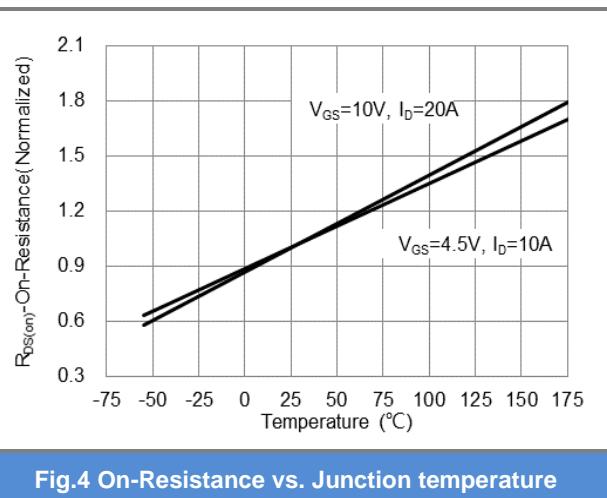


Fig.4 On-Resistance vs. Junction temperature

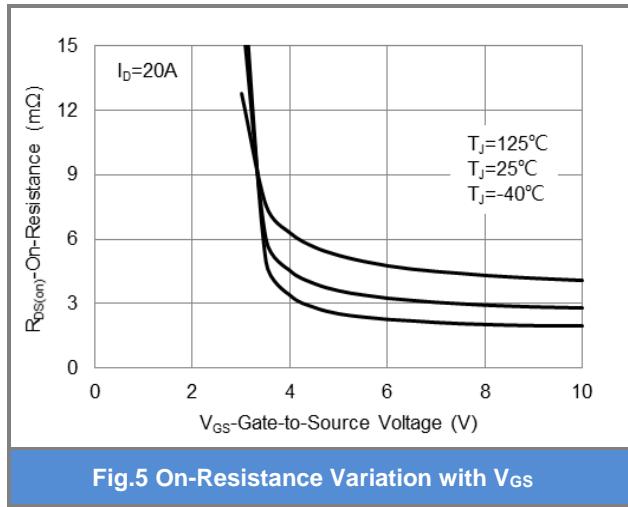


Fig.5 On-Resistance Variation with V_G

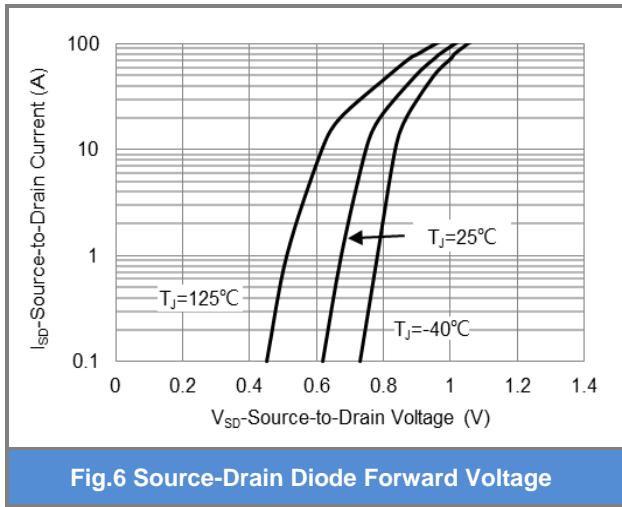


Fig.6 Source-Drain Diode Forward Voltage

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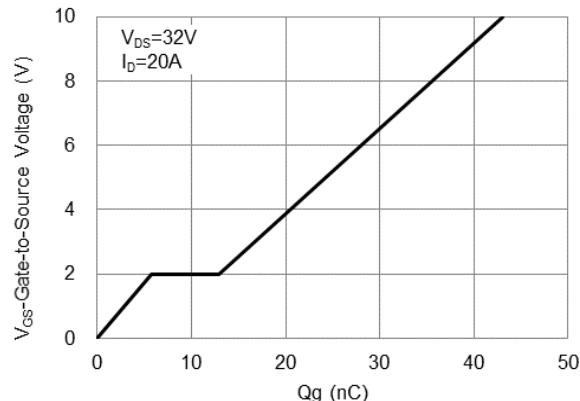


Fig.7 Gate-Charge Characteristics

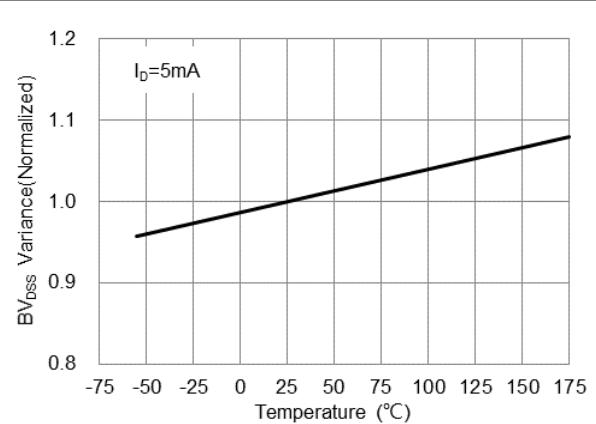


Fig.8 Breakdown Voltage Variation vs. Temperature

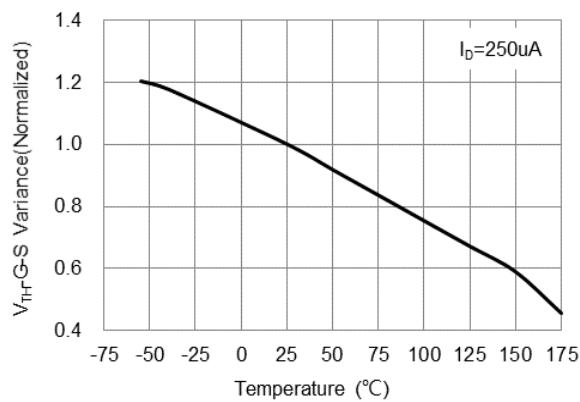


Fig.9 Threshold Voltage Variation with Temperature

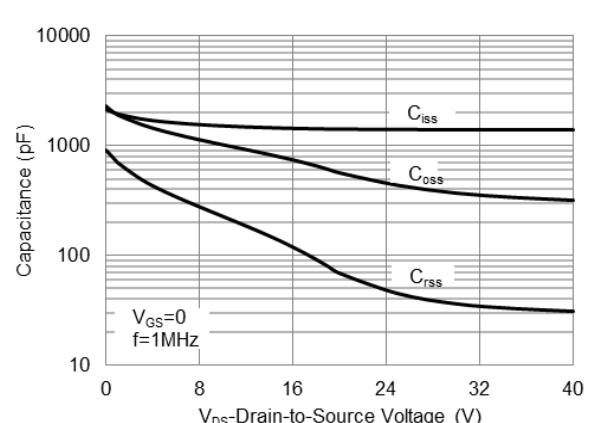


Fig.10 Capacitance vs. Drain-Source Voltage

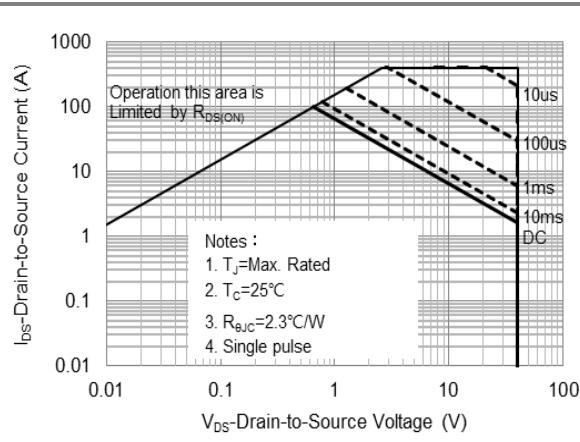


Fig.11 Maximum Safe Operating Area

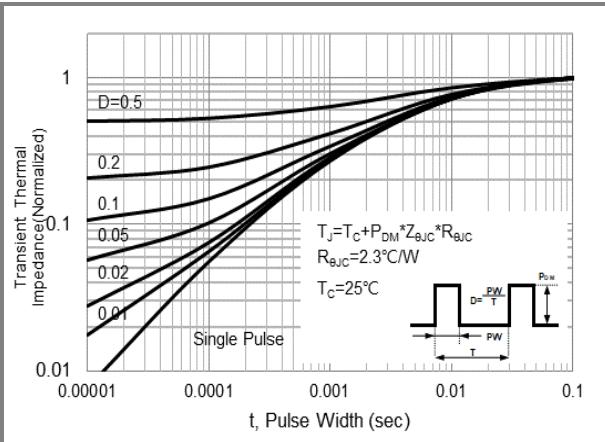


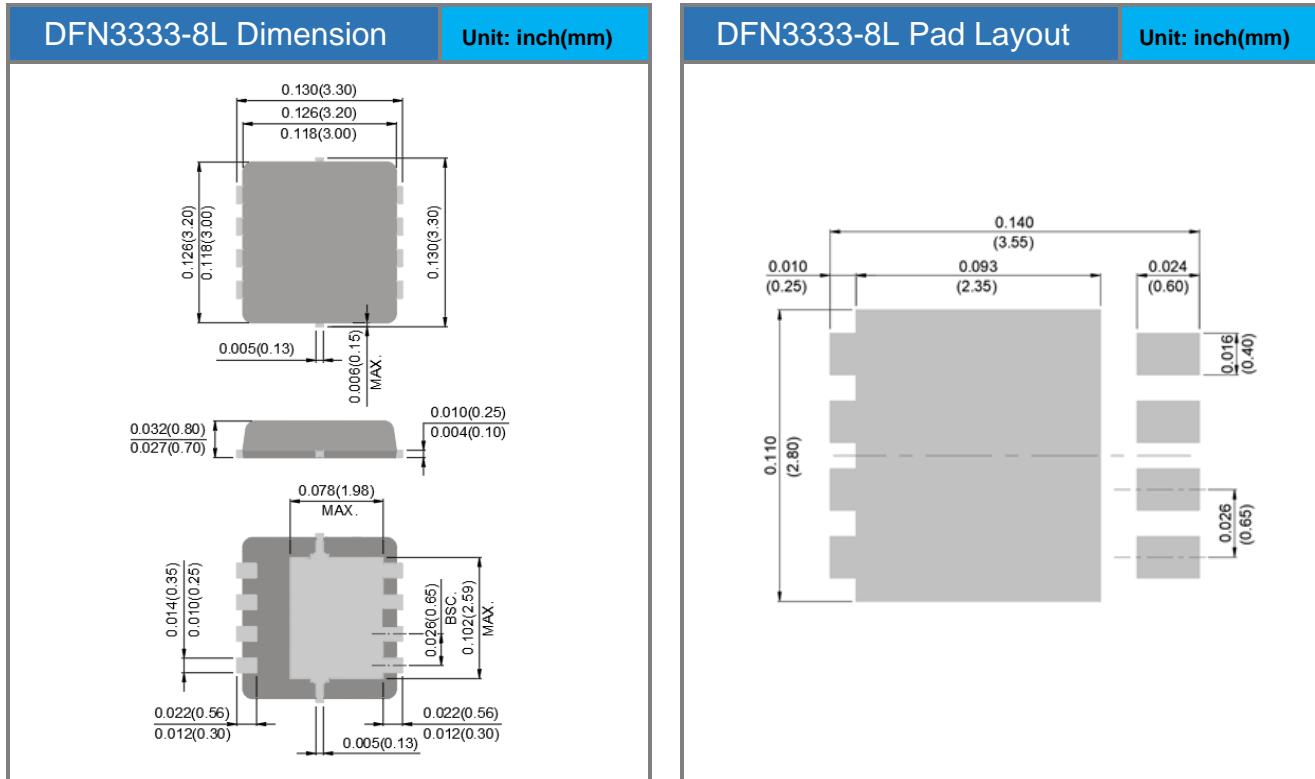
Fig.12 Normalized Transient Thermal Impedance

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ4544S6P-AU	DFN3333-8L	5K pcs / 13" reel	544W

Packaging Information & Mounting Pad Layout



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