PM20025G-08 Datasheet

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Contents

1 Introduction

This document is the datasheet for the PM20025G-08 series. The PM20025G-08 series of chips are motor-specific MCUs developed by MetaWells. They include the following models:

- PM20025G-08 (WQFN6x6-48 package)

Users can refer to the "PM20025G User Manual" for further understanding of the functionality of this series of chips.

2 Product Description

The PM20025G-08 series uses an ARM® Cortex®-M0 core with a maximum operating frequency of up to 48MHz, and is equipped with 32Kbyte of Flash and 4Kbyte of SRAM.

Built-in a 16-bit advanced timer with 3 PWM outputs, all of which have asymmetric dead zone complementary outputs, a 32-bit general-purpose timer, a 16-bit general-purpose timer, and a 16-bit basic timer.

Built-in 1 simple RTC, supports alarm clock function, can run in low power consumption mode, provides a wake-up source for the chip.

Built-in analog circuit includes: 1 12-bit ADC dual-channel simultaneous sampling and protection, as well as up to 10 external channels, 3 analog operational amplifiers with PGA mode, 4 analog comparators with threshold PGA, 1 power-on/power-down/under-voltage reset circuit POR/PDR/BOR, and 1 internal reference voltage for on-chip ADC sampling.

All pins except for power, ground, and NRST can be used as GPIO, peripheral IO, or external interrupt inputs; In applications where the number of pins is limited, provide as many pins as possible.

Support traditional Flash read-write protection, as well as the patented Flash code encryption developed by MetaWells.

Built-in multiple communication interfaces: 2-channel UART, 1-channel high-speed SPI, 1-channel I2C.

It also integrates a hardware division and square root operation unit DVSQ, which improves the software processing capability and the ability to quickly respond to external events.

Support Sleep and Stop low power consumption modes, suitable for applications with high requirements for low power consumption of chips.

Built-in 5V 50mA LDO and 12V LDO control circuits with output short circuit protection.
Built-in three-phase brushless gate driver, capable of operating at up to 36V, is designed to drive MOSFETs with a 6N structure.

With these rich peripherals, PM20025G-08 is particularly suitable for applications such as square wave/FOC drive control for BLDC/PMSM motors：

- Electric tools
- Industrial fans
- Compressors
- Range hoods
- Vacuum cleaners
- Water pumps
- Air conditioners

2.1 Product Features

- **CPU Core**
  - ARM® Cortex®-M0
  - Maximum clock frequency： 48 MHz
  - 24-bit SysTick Timer
- **Operating Voltage Range:**
  - Driver： 5.5V ~ 36V
- **Operating temperature range：**
  - -40℃ ~ +105℃
- **Memory**
  - 32 Kbyte Flash
    - When the CPU's clock frequency is not higher than 24MHz, it supports 0-wait-state bus cycle access to Flash.
    - The Flash has a data security protection feature, allowing separate settings for read protection and write protection.
    - It supports instruction and data encryption for Flash storage, which can prevent the Flash content from being physically attacked.
  - 4Kbyte SRAM
- **Clock**
  - External high-speed HSE clock： 4~32MHz
  - On-chip high-speed HSI clock： 8/12/48MHz
  - On-chip slow-speed LSI clock： 40kHz
  - PLL Clock： 1~48MHz
  - External GPIO input clock： 5~30MHz
- **Reset**
  - External Pin Reset (NRST Pin)
  - Option Byte Loader Reset
  - Window Watchdog Counter Termination (WWDG Reset)
  - Independent Watchdog Counter Termination (IWDG Reset)
  - Power-on Reset (POR/PDR/BOR)
  - Software Reset (SW Reset)
  - Low-Power Management Reset
- **GPIO Port**
  - Supports up to 11 GPIO ports
- **1 DMA Controller**
  - With 5 channels, allowing selection of different request sources.
  - Supports triggering from various peripherals such as TIM, SPI, I2C, UART, ADC, etc.

- **Data communication interfaces**
  - 2 x UART
  - 1 x I2C
    - 1Mbps/400kbps/100kbps transmission Rate
    - Support data reception wake-up in Stop mode
  - 1 route high speed SPI
    - Maximum transmission rate of 18 Mbps
- **Timer**
  - 1 dedicated 16-bit advanced motor control timer (TIM1)
    - 4 PWM outputs, with 3 featuring asymmetric dead-time complementary PWM outputs
    - Support external pin signal braking and internal comparator output signal braking
    - Support multi-point comparison output triggers for ADC on CC1~CC6 channels
  - 2 general-purpose timers
    - 1 x 32-bit general-purpose timer (TIM2)
    - 1 x 16-bit general-purpose timer (TIM3)
  - 1 x 16-bit basic timer (TIM6)
- **DVSQ**
  - Supports 32-bit fixed-point division, providing both quotient and remainder simultaneously
  - Supports high-precision square root calculation for 32-bit fixed-point numbers
- **On-chip analog circuits**
  - 12V LDO Control Circuit
  - 1 x 5V LDO
    - Maximum output voltage of 5.10V
    - Output current of 50mA
  - 1 x 12-bit Dual-Channel Sample-and-Hold SAR ADC (up to 10 external analog signal input channels)
    - 12-bit resolution
    - Maximum conversion frequency: 1MSPS
    - 2 independent sample-and-hold units, capable of sampling two signals simultaneously
    - Support 4 independent conversion queues and 1 test queue
    - Support automatic continuous conversion and scan conversion functions
    - Support channel replacement function in regular queues
    - Support multiple hardware trigger sources (TIM1_TRGO, TIM1_CCx, GPIO input events, etc.)
    - Support averaging of multiple sampled data in regular queues
    - Independent channel data result registers
  - Internal Reference Voltage
    - Internal reference voltage output connected to a dedicated ADC channel

- 4 Voltage Comparators
  - Comparator reference voltage can be from an external signal input or an internal 8-bit DAC
  - Comparator output can be used as a brake for advanced timers
- 3 Operational Amplifiers
  - Gain programmable
  - Amplifier output signal can be routed to a pin or internally to an ADC sampling channel

◆ **Three-phase brushless gate driver**

- Drive Current: +1.5A/-1.8A (typ.)
- Integrated VCC and VBS undervoltage protection
- Floating Absolute Voltage: 70.0V
- Integrated common-mode noise cancellation circuit
- Integrated dead-time: 250ns (typ.)
- Integrated bootstrap diode

◆ **96-bitunique chip ID identifier**

- Used as serial numbers and security keys
- Activates secure boot process

◆ **CPU Tracing and Debugging**

- SWD debug interface
- ARM® CoreSight™ debug components (ROM-Table, DWT, and BPU)
- Custom DBGMCU debug controller (low-power mode emulation control, debug peripheral clock control, debug and trace interface allocation)

2.2 Device Overview

Table 2-1 PM20025G-08 Series Feature

Feature		PM20025G-08
GPIO		30
Package		WQFN6x6-48
Operating Voltage		5.5V~36V
Operating Temperature		-40°C ~ +105°C
Memory	Flash(Kbyte)	32
	SRAM(Kbyte)	4
CPU	Core	Cortex®-M0
	Operating Frequency	48MHz
Number of DMA Channels (DMA Channel Count)		1（5 Channels）
Fixed-Point Division and Square Root Unit (DVSQ)		1
Clock	Internal LSI	40kHz
	Internal HSI	8 MHz /12 MHz /48MHz

Feature		PM20025G-08
	PLL Clock	Supported
	External HSE	4~32MHz
Timer	Advanced Timer	1 个（16 bit）：TIM1
	General Timer	1 个（32 bit）：TIM2 1 个（16 bit）：TIM3
	Basic Timer	1 个（16 bit）：TIM6
	Simple Real-Time Clock (RTC)	1 Independent 32-bit Counter (Capable of Operating in Low-Power Mode)
	System Tick Timer	1
	Independent Watchdog Timer (IWDG)	1
	Window Watchdog Timer (WWDG)	1
Communication Peripherals	UART	2
	I2C	1
	SPI	1
ADC	Number of ADCs (External Analog Channel Count)	1（10）
	Reference Selection	Internal Reference Voltage
	ADC Conversion Rate	1MSPS
	ADC Accuracy	12-bit
Voltage Comparator (COMP)		4
Operational Amplifier (OPAMP)		3
Three-Phase Gate Driver		6N
96-bit UID		1

3 Function Introduction

3.1 Block Diagram

The chip internally integrates a 5V LDO (Low-Dropout Regulator), a 12V LDO control chip, an d a Gate Driver. The internal connection method is as follows:

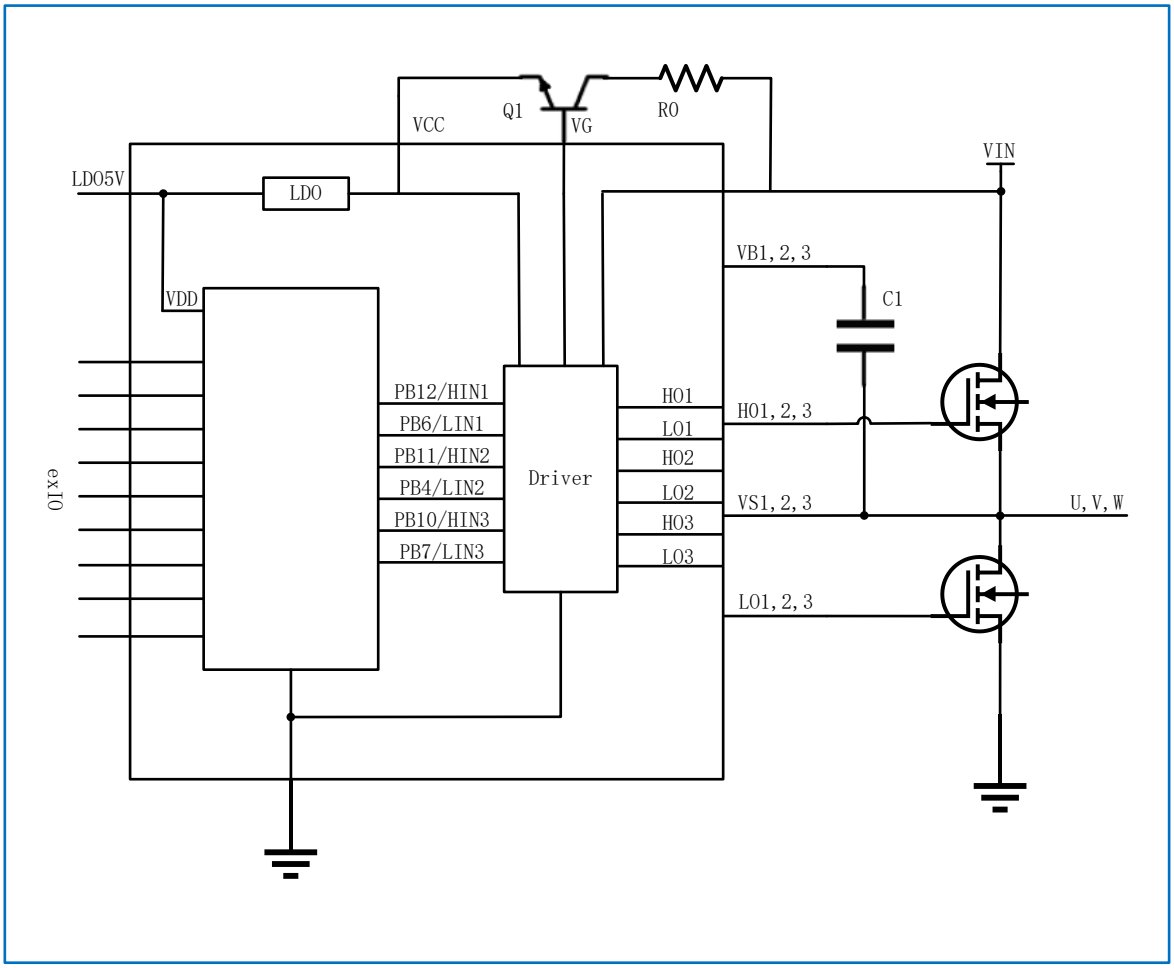

Figure 3-1 PM20025G-08 Block Diagram

Note: When the power supply voltage is within 30V, the reference circuit in Figure 3-1 can be used. If the power supply voltage is above 30V, a separate 12V power supply is required.

3.2 Structural Block Diagram

The device internally integrates 32Kbytes of Flash memory, which is used for storing programs and data.

The ARM® Cortex®-M0 processor is an embedded 32-bit RISC processor that offers excellent computational performance and advanced interrupt system response. This series of products features a built-in Cortex®-M0 core, making it compatible with all ARM tools and software.

Taking PM20025G-08 as an example, the functional block diagram of this series of products is as follows:

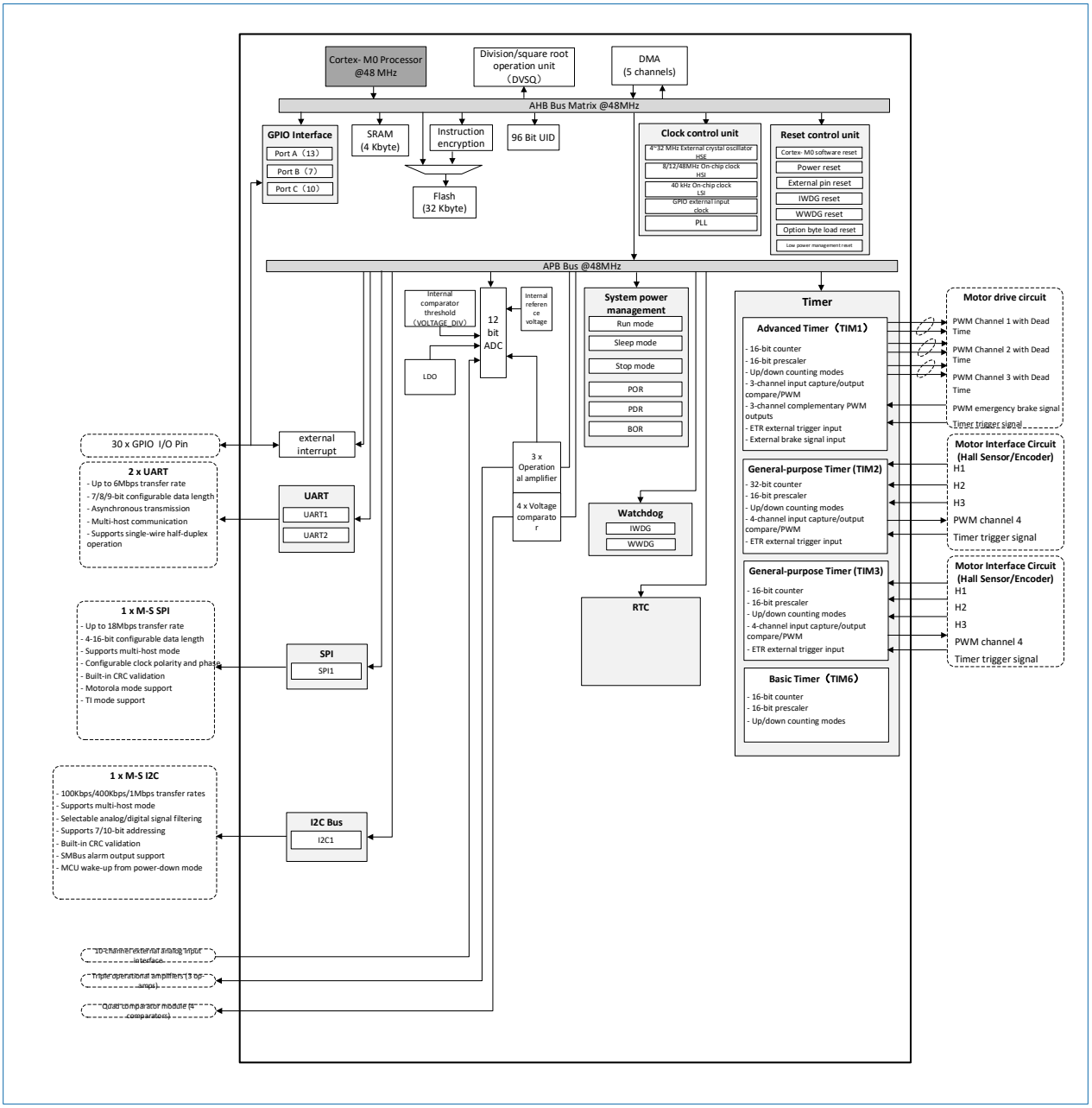

Figure 3-2 PM20025G-08 Functional Block Diagram

3.3 Memory Mapping Configuration

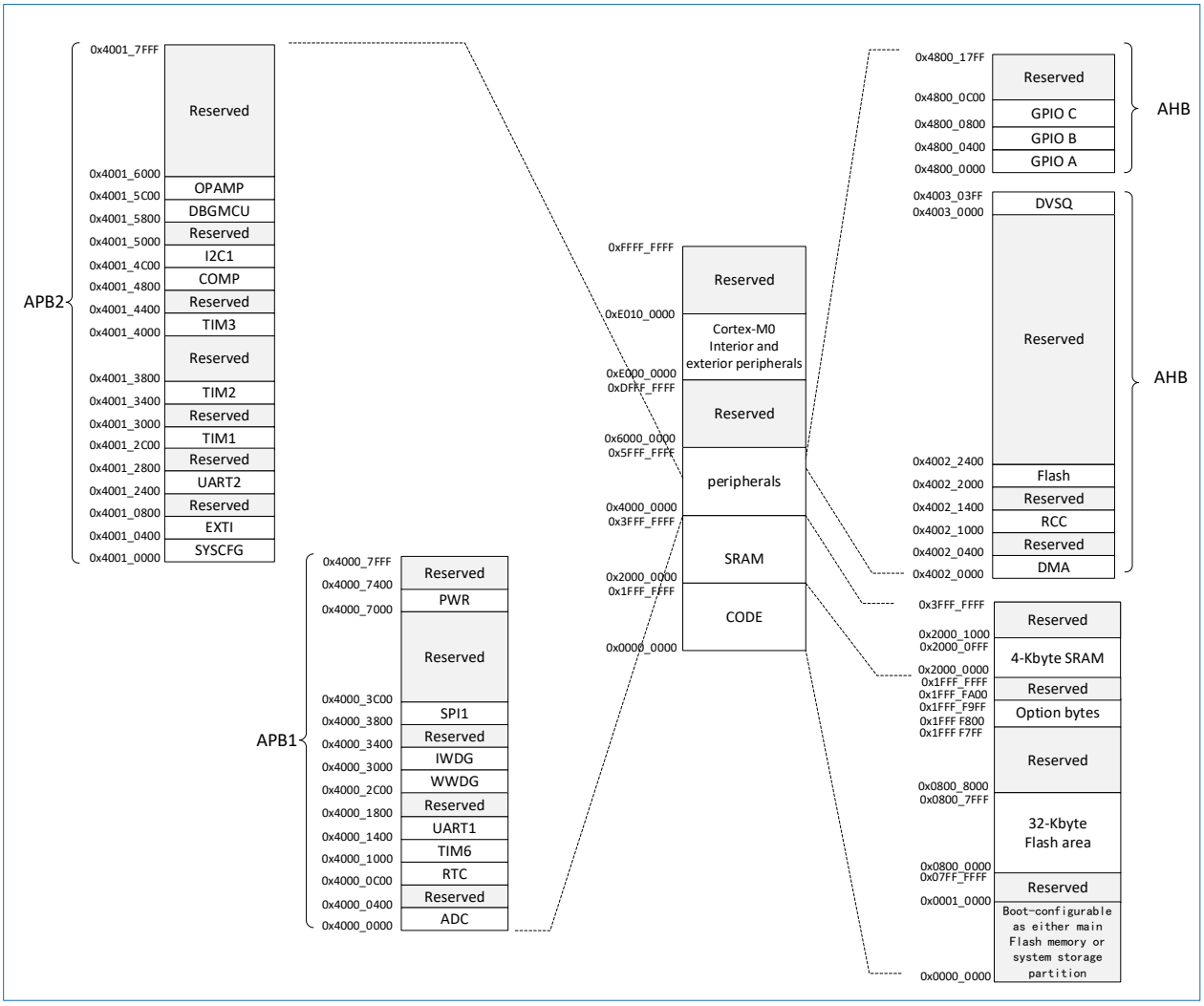

Figure 3-3 PM20025G-08 Memory Mapping

3.3.1 Flash

The series of chips internally integrates up to 32 Kbytes of Flash memory, which is used for storing programs and data.

Through the register configuration of the Flash controller, the remap of interrupt vectors within the 32 Kbyte space can be achieved.

3.3.2 SRAM

The series of chips internally integrates 4 Kbytes of SRAM, supporting word, half-word, and byte read/write access. The CPU can perform fast read/write access with zero wait cycles, meeting the needs of most applications.

3.4 Power Supply

V_{IN} =5.5-36Vwith a 5V LDO outputting power to both internal VDD and VDD_A.

VDD supplies power to the chip's digital circuitry, I/O pins, and internal voltage regulators.

VDD_A powers the analog sections such as ADCs, voltage comparators, and operational amplifiers.

Note：

VDD and VDDA are internally connected together.

3.5 Power Supply Monitor

The chip is equipped with built-in Power-On Reset (POR), Power-Down Reset (PDR), and Brown-Out Reset (BOR) circuits. The system can operate normally when the supply voltage reaches 2.2V. When VDD/VDD_A falls below the specified threshold voltages V_{POR}/V_{PDR}, the system remains in reset state without the need for an external reset circuit. During power-up, the BOR keeps the device in reset state until the power supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, power supply is monitored by POR/PDR.

3.6 Low-Power Modes

The device supports Sleep mode and Stop mode.

Sleep Mode: Only the CPU stops, while all peripherals remain operational and can wake up the CPU upon occurrence of an interrupt/event.

Stop Mode: Stop mode achieves the lowest power consumption while preserving SRAM and register contents. In stop mode, all clocks in the core domain are turned off, and PLL, HSI, and HSE oscillators are disabled. The MCU can be woken up from stop mode by any signal configured as EXTI, which can be one of the 16 external I/O ports. The MCU can also be woken up from Stop mode after receiving data via I2C.

3.7 Reset

3.7.1 System Reset

System reset resets all registers to their reset states, except for the reset flag bits in the RCC_CSR register. Users can identify the source of the reset event by checking the reset status flag bits in the RCC_CSR control and status register.

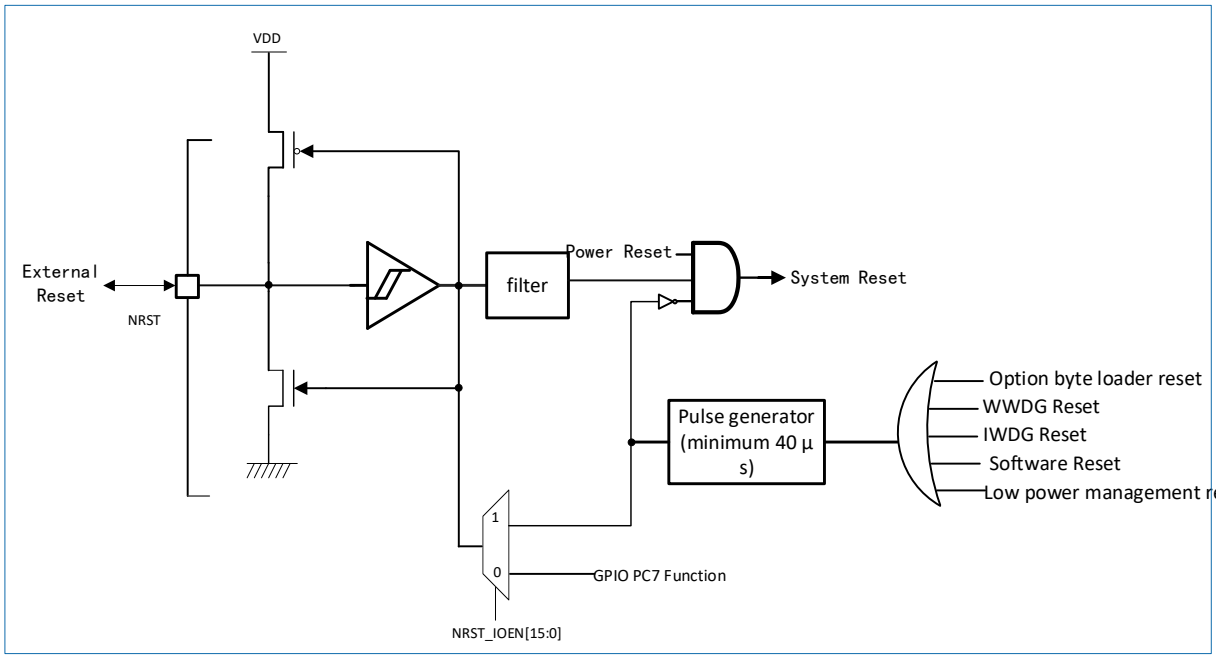

Figure 3-4 Reset Signal

When any of the following events occur, a system reset will be generated:

- Low level on the NRST pin (external reset)
- Option byte loader reset
- Window watchdog timer counter expiration (WWDG reset)
- Independent watchdog timer counter expiration (IWDG reset)
- Power reset (power-on reset/power-down reset/brown-out reset)
- Software reset (SW reset): This can be achieved by setting the SYSRESETREQ bit in the Cortex®-M0 Interrupt Enable and Reset Control Register to '1'.
- Low-power management reset

Except for power resets, all other reset sources will ultimately act on the NRST pin and remain low during the reset process. The reset entry vector is fixed at address 0x00000004. The internal reset signals within the chip (excluding power resets) will be output on the NRST pin. The pulse generator ensures that each internal reset source has a pulse delay of at least 40 microseconds. When the NRST pin is pulled low to generate an external reset, a reset pulse will be generated.

3.7.2 Power Reset

A power reset will be generated when any of the following events occur:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

The chip integrates an internal power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always active to ensure the system operates normally when the power supply exceeds 2.2V. When VDD is less than the POR/PDR threshold, the MCU will be reset without the need for an external reset circuit.

The chip also integrates an internal brown-out reset (BOR) circuit. The BOR option is not

enabled by default, and the power supply is monitored by the POR/PDR at this time. Users can configure the MCU option bytes to enable or disable the BOR function.

3.8 Clock & Clock Tree

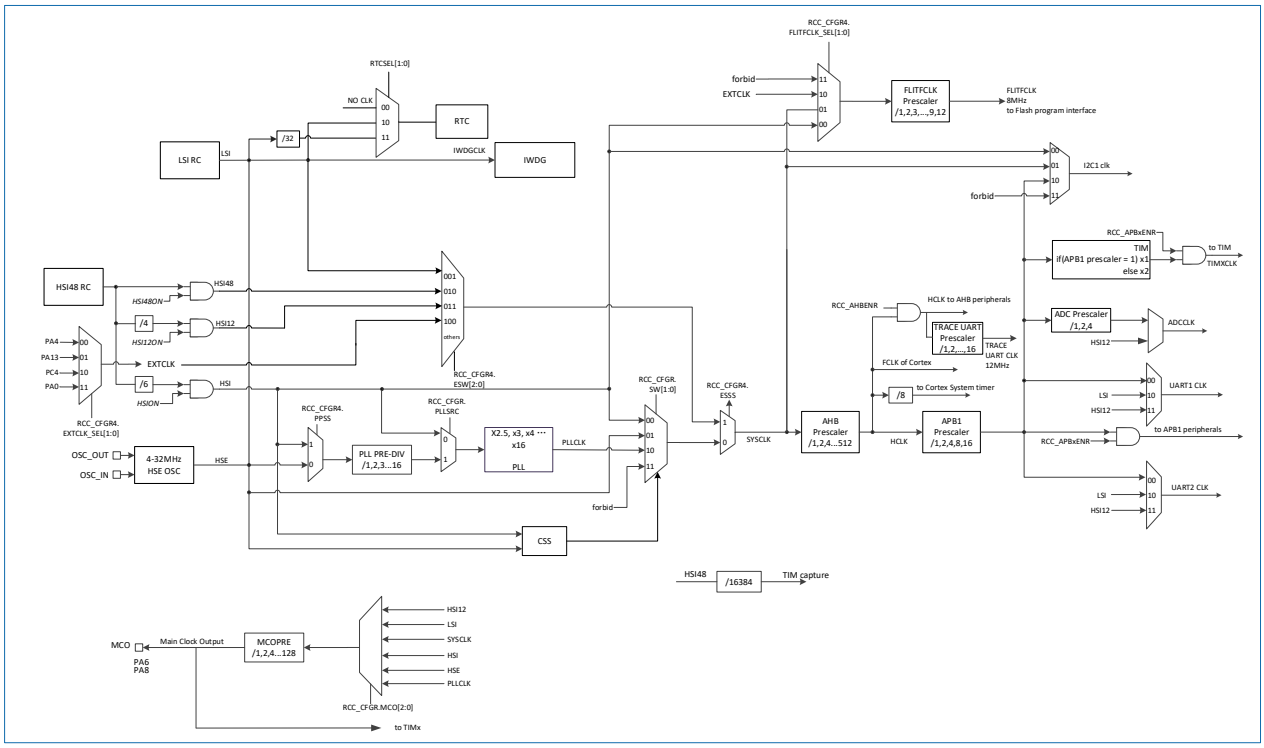

Figure 3-5 Clock Tree

As shown in the diagram above, HSI48 and ADCCLK are derived from the same internal oscillator with an output frequency of 48MHz. Therefore, when using either the HSI48 or ADCCLK clock, the other clock source cannot be turned off to reduce power consumption.

Upon startup, the device selects the system clock (SYSCLK) as the CPU operating clock. The 48MHz clock output by the internal oscillator is divided down to produce HSI, which serves as the default system clock after the chip is powered on. HSI/HSE can be used as the input for the PLL prescaler, so by using the PLL in combination, a richer variety of system clock frequencies can be configured.

The device provides more clock sources for the system clock, offering customers lightweight, flexible, and diverse working modes. The following clocks can all serve as the system clock:

- External high-speed clock (HSE): 4~32MHz
- Internal high-speed clock (HSI): 8/12/48MHz
- Internal low-speed clock (LSI): 40kHz
- PLL clock: up to 48MHz
- GPIO external input clock: 5~30MHz

The clock frequencies of the AHB bus and APB domain can be configured through several dividers. The maximum clock frequency of the AHB bus can reach 48MHz, and the maximum clock frequency of the APB domain can also reach 48MHz.

The Clock Security System (CSS) can monitor failures of the HSE and switch clock sources when

a failure is detected.

3.9 GPIO

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (floating, pull-up, or pull-down), or as another peripheral function port. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have high-current carrying capability. When necessary, the peripheral function of an I/O pin can be locked through a specific operation to avoid accidental writes to the I/O registers.

3.10 SYSCFG

This series of chips includes a set of system configuration registers. The main functions of the System Configuration Controller are as follows:

- Enable or disable I2C Fast Mode Plus on some IO ports.
- Remap memory to the code start area.
- Manage external interrupts connected to GPIO ports.
- Manage TIM3_CH4 input remapping to signals such as LSI, HSI, etc.
- Manage the switching of some internal analog signals to IO.
- Configure the internal voltage divider (8-bit DAC).

3.11 Boot Mode

During startup, the boot pins are used to select one of the following boot modes:

- Boot from user Flash
- Boot from system memory

The bootloader is stored in system memory and can be used to reprogramming the Flash via UART1 (PC8/PC9).

3.12 DMA

The Direct Memory Access Controller (DMA) is responsible for high-speed data transfer between peripherals and memory or between memories. Data is quickly moved from the source address to the destination address without CPU involvement, allowing the CPU to have more resources to handle other applications.

The chip integrates one DMA controller. The DMA controller manages access requests from one or more peripherals. The DMA has an arbiter to handle requests with different DMA priorities.

- The DMA has 5 independently configurable channels.
- Each channel is connected to specific hardware and triggered by that hardware or by software.
- Supports circular buffer management.

- Supports DMA request mapping for TIM1/2/3, SPI1, UART1/2, I2C1, and ADC.

3.13 Interrupts and Events

3.13.1 NVIC

This series of MCUs includes a built-in Nested Vectored Interrupt Controller (NVIC) capable of handling up to 22 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and 4 interrupt priorities. This module provides flexible interrupt management functionality with minimal interrupt latency.

- The tightly coupled NVIC enables low-latency interrupt response processing.
- Interrupt vector entry addresses directly into the core.
- Allows early processing of interrupts.
- Handles late-arriving higher-priority interrupts.
- Supports interrupt tail-chaining functionality.
- Automatically saves processor state.
- Automatically restores upon interrupt return without additional instruction overhead.

3.13.2 EXTI

The Extended Interrupt and Event Controller (EXTI) is responsible for managing asynchronous interrupts and events: outputting event requests to the CPU, outputting interrupt requests to the interrupt controller, and outputting wakeup requests to the power management module.

EXTI can be divided into two types based on whether the interrupt/event trigger edge is configurable: configurable EXTI (simply called configurable EXTI) and fixed EXTI (simply called fixed EXTI). Fixed EXTI uses rising edge triggering and only works in standby mode to wake up the core from standby mode.

- Support up to 22 event/interrupt requests.
  - 22 configurable EXTI lines
  - Trigger edge selectable as rising or falling
  - Has dedicated interrupt status bits
  - Can trigger interrupts and events via software
  - 1 fixed EXTI line
- Each interrupt/event line can be individually triggered and masked.
- Detects external signals with pulse widths lower than the APB2 clock width.

3.14 Independent Watchdog（IWDG）

The Independent Watchdog is clocked by an internal, independent 40kHz RC oscillator (LSI) and includes a 12-bit down-counter and an 8-bit prescaler. Since this RC oscillator is independent of the main clock, it can operate in standby mode. The IWDG is used to reset the entire system in

case of problems or as a free-running timer to provide timeout management for applications. It can be configured as software or hardware-started watchdog through option bytes. In debug mode, the counter can be frozen.

By configuring the IWDG_WINR register, the IWDG can operate in window mode.

3.15 Window Watchdog （WWDG）

The Window Watchdog includes a 7-bit down-counter. The counter can be set to free-running mode or used as a watchdog to reset the entire system in case of system failure. The Window Watchdog is driven by the main clock and has an early warning interrupt function. In debug mode, the counter can be frozen.

3.16 Timer

This series of MCUs includes one advanced control timer, two general-purpose timers, and one basic timer. The timer functions are defined in the table below.

Table 3-1 Definition of Timer Function

Type	Timer Name	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Emergency Brake Input	Capture/ Comparative Channel	Complementary Output
Advanced timer	TIM1	16 bit	Increment, decrement, increment/decrement	1~65536	Yes	Yes	3	3
General timer	TIM2	32 bit	Increment, decrement, increment/decrement	1~65536	Yes	No	4	No
	TIM3	16 bit	Increment, decrement, increment/decrement	1~65536	Yes	No	4	No
Basic Timer	TIM6	16 bit	Increment,	1~65536	No	No	No	No

3.16.1 Advanced Timer

This series of MCUs integrates an advanced timer TIM1.

The TIM1 advanced timer can be used as a three-phase PWM generator with six channels, as well as a complete general-purpose timer. TIM1 has three independent channels that can be used for:

- Input capture
- Output comparison
- Generates PWM edge or center alignment patterns
- Single pulse output

- Complementary PWM output with programmable dead-time insertion.

When the advanced timer is configured as a 16-bit conventional timer, it has the same functionality as the basic timer. When configured as a 16-bit PWM generator, the advanced timer has full modulation capability of 0-100%. Due to the same internal structure and most functions as the general timer, the advanced timer can operate in conjunction with the general timer through the timer link function to provide synchronization or event linking functions.

The advanced timer has a shift function for updating events and a simple data movement function, which can be applied to motor control.

In debug mode, the counter can be frozen.

3.16.2 Universal Timer

This series of MCUs integrates the following two general-purpose timers.

TIM2 and TIM3

The TIM2 general-purpose timer is based on a 32-bit auto-reload increment/decrement counter and a 16-bit prescaler. The TIM3 general-purpose timer is based on a 16-bit auto-reload increment/decrement counter and a 16-bit prescaler. Both TIM2 and TIM3 have four independent channels. These channels are used for input capture/output comparison, PWM, or single pulse mode output.

TIM2 and TIM3 general-purpose timers can work in conjunction with TIM1 advanced control timers through timer linking functions to provide synchronous or event linking capabilities. Both TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 are capable of processing quadrature incremental encoder signals and also handling the digital outputs from 1 to 3 Hall-effect sensors. In debug mode, its counters can be frozen.

3.16.3 Basic Timer

This series of MCUs integrates a basic timer TIM6.

The TIM6 basic timer is based on a 16-bit auto-reload incrementing counter and a 16-bit prescaler. In debug mode, its counters can be frozen.

3.16.4 System Tick Timer

The System Tick timer is dedicated to the operating system and can be used as a standard decrement counter. It has the following characteristics.

- 24-bit down counter
- reload function
- When the counter is 0, a maskable interrupt can be generated
- Programmable clock source

3.17 ADC

Built-in 1 12-bit analog/digital converter ADC module with up to 10 external channels and 6 internal channels. The A/D conversion of different channels can be performed in single, cyclic,

intermittent, or scanning sampling modes.

- 12-bit resolution.
- ADC clock can reach 24MHz, and ADC conversion rate can reach 1MSPS.
  Two independent sample and hold units, with inputs from 14 analog input channels.
- ADC supports DMA operation.
- Flexible queue configuration, supporting 4 independent conversion queues and 1 test queue.
- The working mode of the queue supports single-channel acquisition and protection mode, dual-channel acquisition and protection mode, single-channel acquisition and protection scanning mode, and BK mode.
- Flexible arbitration mechanism, each queue can be configured with 0-3 levels of priority, with higher numbers indicating higher priority.
- Independent result registers: Each channel has its own independent result register, which can store the current conversion value.
- Channel replacement feature allows redirecting channel conversion requests to other channels. This feature can be used to measure the same input channel and store the conversion results in multiple different result registers.
- Data window comparison function, which can compare the data converted by ADC with the set value.
- Data averaging function, where the data averaging unit performs data preprocessing.
- Trigger Trig delay configuration, which can be configured to delay for a period of time after the trigger signal is generated before starting the ADC conversion.
- Events generated by the advanced control timer TIM1 and the general-purpose timers TIM2/3 can be internally connected to the ADC's start trigger to trigger A/D conversion.

3.17.1 Internal Reference Voltage

The internal reference voltage VREFINT provides a stable bandgap reference voltage output for the ADC.

3.18 Voltage Comparator（COMP）

This series of chips has four low-power comparators COMP1, COMP2, COMP3, and COMP4 built in. These four comparators can be used as independent devices or in combination with timers.

These four comparators can be used for:

- Wake up the MCU from low power consumption mode triggered by analog signals.
- Conditioning analog signals.
- When used in conjunction with the PWM output of the timer, it constitutes a cycle-by-cycle current control loop.

3.19 Operational Amplifier（OPAMP）

The device integrates three operational amplifiers, hereinafter referred to as "op-amps".

They can work in three modes: Standalone, Follower, and PGA.

The output of the operational amplifier can be output to the pin, can be internally fed back to the inverting input terminal, or can be gated and input to the internal ADC for sampling.

3.20 Division and Square Root Calculation Unit（DVSQ）

Division and square root, DVSQ calculation unit supports the following features:

- Support 32-bit signed number SDIV and unsigned number division UDIV, and supports 32-bit square root operation.
  - At the same time, the DVSQ calculation unit cannot support both division and square root operations simultaneously, and can only perform one of the two operations.
  - After the division operation of a 32-bit signed/unsigned integer, the quotient and remainder can be obtained simultaneously and updated to the corresponding registers.
  - Division supports the MOD operation.
- Unsigned square root operation, which can be selected for high-precision square root operation through software.
- Pipeline design, each clock completes 2-bit operation.
- The computation time varies depending on the data being processed.
- Supports zero-based interrupt and overflow interrupt.

3.21 I2C Bus

The series of MCUs has one I2C bus interface, which can work in multiple master and slave modes, supporting standard mode up to 100kHz, fast mode up to 400kHz, and ultra-fast mode up to 1MHz.

I2C provides hardware support for SMBUS2.0 and PMBUS1.1: ARP capability, host notification protocol, hardware CRCPEC generation/validation, timeout validation, and ALERT protocol management.

I2C also has a clock independent of the CPU clock domain, so that I2C can wake up the MCU from the Stop mode when the address matches.

Table 3-2 I2C Features

I2C Features	I2C1
Master/Slave Mode	Supported
Multi-Master Mode	Supported
Standard/Fast/Super Fast Mode	Supported
7/10 bit Addressing Mode	Supported
Broadcast Call	Supported

I2C Features	I2C1
Event Management	Supported
Clock Stretching	Supported
Software Reset	Supported
DMA Transfer (Direct Memory Access Transfer)	Supported
Digital and Analog Filters	Supported
SMBUS2.0	Supported
PMBUS1.1	Supported
Independent Clock	Supported
Wake-up from Slave Halt Mode	Supported

3.22 Universal Asynchronous Receiver/Transmitter (UART)

The device is equipped with two Universal Asynchronous Receiver/Transmitters (UART1/UART2), with a maximum communication rate of up to 6Mbit/s. It provides hardware management for RS485DE signals, multi-processor communication mode, and single-wire half-duplex communication mode.

The UART interface can utilize a DMA controller.

Table 3-3 UART Features

UART Mode/Feature	UART1/UART2
Data Word Length	7/8/9 bit
Direct Memory Access (DMA) Transfer	Supported
Multiprocessor Communication	Supported
Single-Wire Half-Duplex Communication	Supported
RS232 Hardware Flow Control	Not Supported
RS485 Driver Enable	Supported

3.23 Serial Peripheral Interface (SPI)

This series of MCUs features up to one SPI interface, supporting both slave and master modes, as well as full-duplex and half-duplex communication modes. The SPI can utilize a 3-bit prescaler to generate 8 different master mode frequencies, and each frame can be configured with data lengths ranging from 4 bits to 16 bits.

Table 3-4 SPI Feature

SPI Feature	SPI1
Hardware CRC Calculation	Supported
RX/TX FIFO	Supported
NSS Pulse Mode	Supported
TI Mode	Supported

SPI Feature	SPI1
DMA Transfer	Supported

3.24 RTC

The RTC features a set of continuously running counters that can provide clock functionality through software. It also has alarm interrupt and second interrupt capabilities (both can serve as wakeup sources in standby mode).

The driving clock for the RTC can be selected from either HSE/32 or LSI. The RTC includes a 32-bit programmable counter that, in conjunction with the alarm register, can perform long-duration measurements and generate alarm events.

3.25 96-bit UID

The 96-bit Unique Identifier (UID) provides a reference number that is unique to every MetaWells chip, regardless of the circumstances. Users cannot modify this identifier. Depending on the application, the 96-bit UID can be read in units of bytes (8 bits), half-words (16 bits), or full words (32 bits). The 96-bit UID is suitable for:

- Serving as a serial number (e.g., for USB character serial numbers or other terminal applications).
- Serving as a password. When programming flash memory, combining this UID with software encryption and decryption algorithms can enhance the security of the code within the flash memory.
- Activating the bootstrap process with security mechanisms.

3.26 Debug Interface（DBG）

The embedded ARM SWJ-DP interface enables the implementation of a serial SWDIO/SWCLK debug interface.

3.27 LDO

Internally integrated is a 12V LDO control circuit that, paired with external circuitry, provides a 12V voltage to the 5V LDO. The output of the 5V LDO is used to power the MCU.

3.28 Three-Phase Gate Drive

The internal driver comprises three independent 70V-tolerant half-bridge gate drives. Figure 3-5 depicts the functional block diagram of the driver, which includes bootstrap diodes and built-in undervoltage lockout (UVLO) protection for both low-side and high-side power supplies to prevent the power tubes from operating at excessively low voltages, thereby enhancing efficiency. The integrated anti-shoot-through dead time is 250ns, with a drive capability of +1.5A/-1.8A. The integrated common-mode noise cancellation technology enables the high-side driver to operate stably in high dv/dt noise environments and possesses a broad negative

transient voltage tolerance.

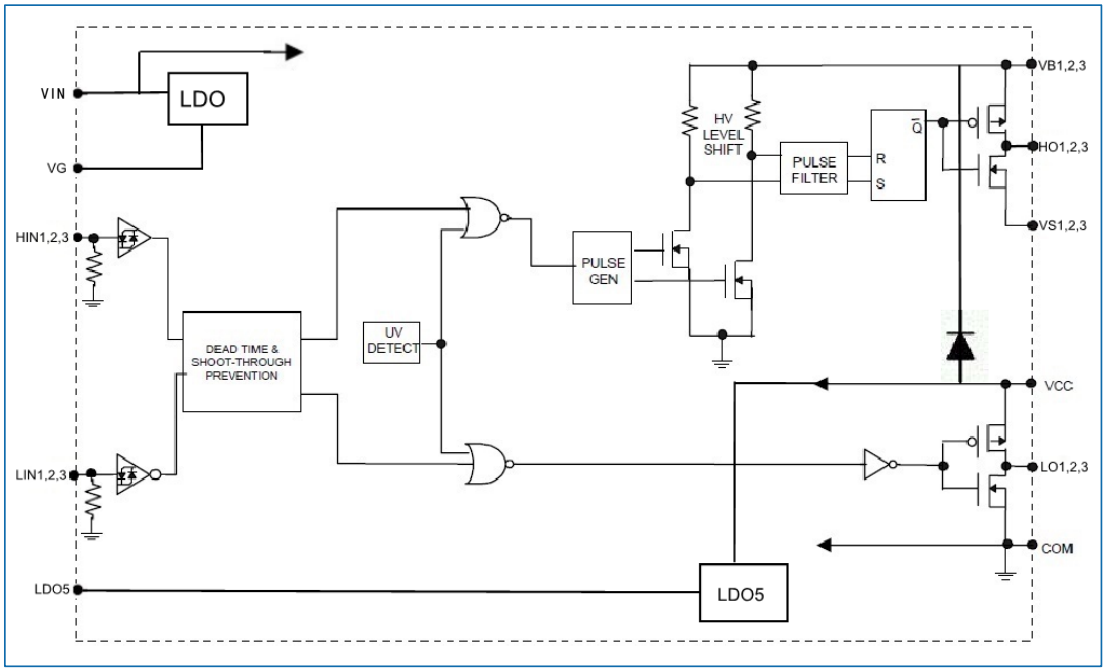

Figure 3-7 Driver Functional Block Diagram

3.28.1 Low-side Power Supply VCC and Under-voltage Lockout（UVLO）

The VCC is the low-side circuit power supply terminal, which provides the required driving energy for the input logic circuit and low-side output power stage operation. The built-in undervoltage lockout circuit ensures that the chip operates within a sufficiently high power supply voltage range, thereby preventing damage to MOSFET/IGBT caused by thermal dissipation due to low drive voltage. As shown in Figure 3-6, when VCC rises and exceeds the threshold voltage VCC_R =3.6V, the low-side control circuit unlocks and starts to work, and LO starts to output; Conversely, when VCC drops below the threshold voltage VCC_F =3.3 V, the low-side circuit locks, the chip stops working, and LO stops outputting. The recommended operating voltage range for VCC is 4.5V-15.0V.

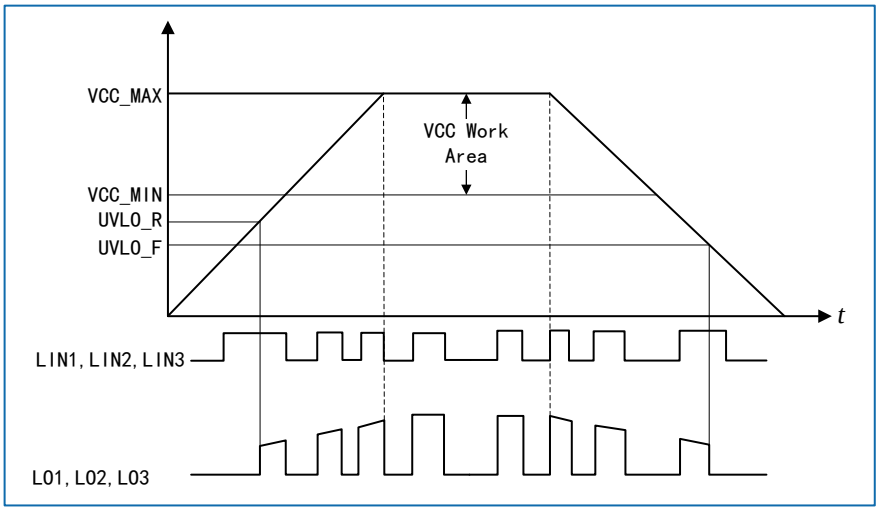

Figure 3-8 Low-side Power Supply VCC and Under-voltage Lockout

3.28.2 High-side Power Supply VBS (VB1-VS1, VB2-VS2, VB3-VS3) and Under-voltage Lockout (UVLO)

The VBS power supply serves as the high-side circuit power source, with VBS1 (VB1-VS1), VBS2 (VB2-VS2), and VBS3 (VB3-VS3) corresponding to the high-side drive power supplies for phases 1, 2, and 3, respectively. The entire high-side circuit powered by the floating power supply VBS uses ground GND as its reference point and follows the source/emitter voltage of the external power transistors MOSFET/IGBT, swinging between ground and bus voltage. Due to the low quiescent current consumption of the high-side circuit, the entire high-side circuit can be powered by bootstrap circuit technology connected to VCC, and only a small capacitor is needed to maintain the voltage required to drive the power transistors. As shown in Figure 3-7, the under-voltage lockout for the high-side power supply VBS is similar to that of the low-side VCC power supply. The recommended operating voltage range for VBS is 4.5V-15.0V.

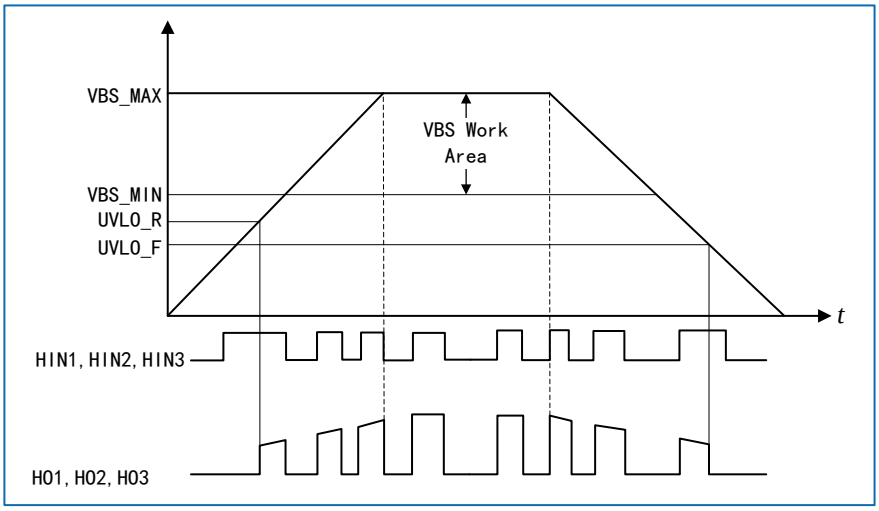

Figure 3-9 High-side Power Supply VBS and Under-voltage Lockout

3.28.3 Low-side and High-side Logic Input Control: HIN&LIN (HIN1,2,3/LIN1,2,3)

In order to better compatible with various controllers, the internal Driver adjusts the threshold of the 6 input Schmitt inverters to the lowest level compatible with 3.3V LSTTL and CMOS logic levels. The built-in Schmitt inverter and advanced pulse filter effectively shield abnormal input short pulse signals, greatly improving the system's immunity to interference and reliability. Each logic input terminal is preset with a 140kΩ pull-down resistor inside the chip to ensure that it can provide a control signal to turn off the power transistor in abnormal situations such as soldering defects and invalid input connections. The input pulse width should be no less than 300ns to ensure the correct input and output relationship.

3.28.4 Shoot-Through Prevention

The internal Driver is equipped with a protection circuit specifically designed to prevent power tubes from being directly connected, effectively preventing power tube damage caused by common mode interference with high-side and low-side input signals. Figure 3-8 shows how the straight-through protection circuit protects the power tube. The power tube is directly connected means that the high-side gate driver output HO and the low-side gate driver output LO in the same half bridge are simultaneously "high", which will cause a very large harmful current to flow through the upper and lower power tubes at the same time, accompanied by a large power loss,

which can directly damage the power tube in severe cases. As shown in Figure 3-7, when the low-side input LIN and high-side input HIN of the same phase are both "high", the internal protection circuit pulls the driver outputs HO and LO to "low", effectively turning off the power transistor. When one of the input signals becomes "low", the driver output needs to undergo a dead time delay before outputting "high". This measure avoids the excessive switching state of the power tube caused by harmful short input pulses, effectively reduces losses, and reduces the risk of damage to the power tube.

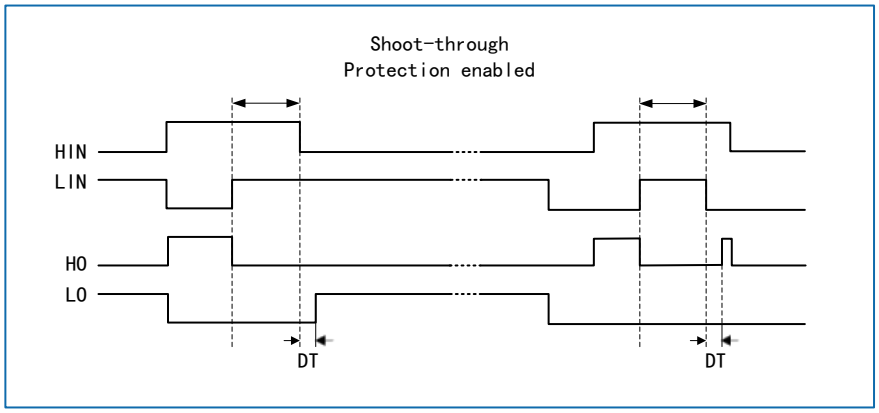

Figure 3-10 Shoot-Through Prevention

3.28.5 Dead Time

The internal Driver is equipped with a fixed dead-time protection circuit. During the dead-time, both the high-side and low-side driver outputs are set to "low." The set dead-time must ensure that one power transistor is effectively turned off before the other is turned on, thus preventing the simultaneous conduction of the upper and lower transistors, known as shoot-through. If the external dead-time set by the logic input is less than the internal minimum dead-time, the dead-time for the driver output will be the one set internally within the chip. Conversely, if the external dead-time set by the logic input is greater than the internal dead-time, the driver output will adhere to the external dead-time set by the logic input. Figure 3-9 illustrates the timing relationship between the dead-time, input signals, and driver output signals.

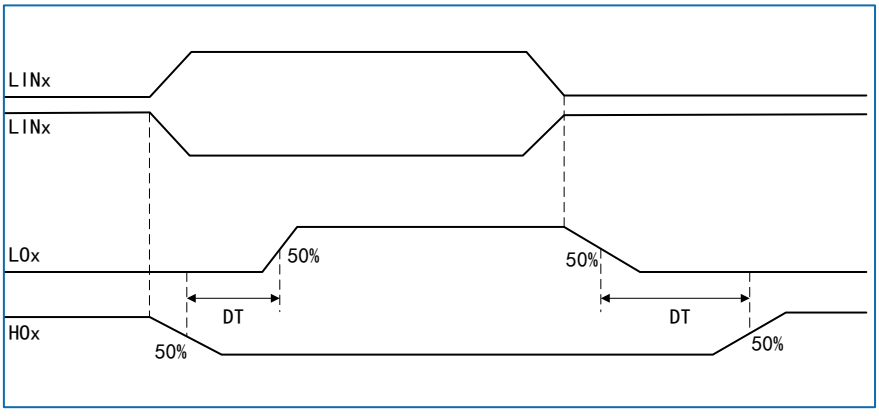

Figure 3-11 Dead Time

4 Electrical Characteristics

4.1 Maximum Absolute Ratings

The maximum rated value is only a short-term pressure value.

Notes：

- Do not operate the chip at this value or any other conditions exceeding the recommended values.
- Refer to Tables 4.1 to 4.18 for the maximum rated values of the chip. Exceeding the maximum rated values may result in permanent damage to the chip.
- Operating for prolonged periods at maximum rated values may affect the chip's reliability.

4.1.1 Limit Voltage Characteristics

Table 4-1 Limit Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{IN}	Voltage Range	-0.3	55	V
High-side Floating Supply Voltage	VB1,VB2,VB3,	-0.3	70.0	
High-side Floating Ground Voltage	VS1,VS2,VS3	VB–20	VB+0.3	
V_{HO}	V_{HO1},V_{HO2},V_{HO3}	VS-0.3	VB+0.3	
V_{LO}	V_{LO1} ,V_{LO2},V_{LO3}	-0.3	V_{CC}+0.3	
V_{IO}	Input Voltage on the Pin	-0.3	5.5	

4.1.2 Extreme Current Characteristics

Table 4-2 Extreme Current Characteristics

Symbol	Description	Maximum	Unit
I_{OHL}	Peak Output Current of Low/High-side Upper Transistor	1.5	A
I_{OLL}	Peak Absorption Current of Low/High-side Upper Transistor	1.8	A
I_{LDO5}	5V LDO Output Current	50	mA
I_{VDD}	Total Current Through VDD/VDD_APower Lines (Supply Current)(1)	105	
I_{VSS}	Total Current Through V_{SS} Ground Lines (Outflow Current) (1)	105	
I_{IO}	Output Sink Current on Any I/O and Control Pin	60	
	Output Source Current on Any I/O and Control Pin	60	

Symbol	Description	Maximum	Unit
$I_{INJ(PIN)}$ (2)	Injection Current on Pin (3)	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total Injection Current on All I/O and Control Pins (4)	-25/+0	

(1). All power（VDD，VDD_A）and ground（V_{SS}，V_{SSA}）pins must always be connected to an external power supply system within the allowable range.

(2). Reverse injection current can interfere with the analog performance of the device.

(3). When V_{IO} >VDD, there is a forward injection current; When V_{IO} < V_{SS}, there is a reverse injection current. The absolute value of the injection current must not exceed the specified range.

(4). When several I/O pins have injection currents simultaneously, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward and reverse injection currents.

4.1.3 Limit Temperature Characteristics

Table 4-3 Limit Temperature Characteristic

Symbol	Description	Minimum	Maximum	Unit
T_{STG}	Storage temperature range	-40	125	°C
T_J	Maximum junction temperature	-40	125	°C

4.2 Operating Parameters

4.2.1 Recommended Operating Conditions

Table 4-4 Recommended Operating Condition

Symbol	Description	Minimum	Maximum	Unit
V_{IN}	Power supply voltage range	5.50	36	V
V_{LDO5}	5V LDO output voltage range	4.80	5.10	V
I_{LDO5}	5V LDO output current range	-	50	mA
V_{HO}	V_{HO1},V_{HO2},V_{HO3}	VS-0.3	VB+0.3	V
V_{LO}	V_{LO1} ,V_{LO2},V_{LO3}	-0.3	15	V
f_{PCLK2}	Internal APB2 Clock Frequency	-	48	MHz
f_{PCLK1}	Internal APB1 Clock Frequency	-	48	
f_{PCLK2}	Internal APB2 Clock Frequency	-	48	
VDD	Standard Operating Voltage	2.2	5.5	V

Symbol	Description	Minimum	Maximum	Unit
V_{REFP} (1)	Analog Operating Voltage	2.2	5.5	V
T	Operating Temperature	-40	105	°C

(1). VDD and V_{REFP} are Internally Connected.

4.2.2 BOR Characteristics

Table 4-5 BOR Characteristics

Symbol	Parameter	Gear	Minimum	Typical	Maximum	Unit
V_{BOR}(1)	BOR Detection Level Selection (VDD Rising Edge) (-40°C ~105°C)	V_{BOR0}	2.34	2.42	2.46	V
		V_{BOR1}	2.75	2.83	2.91	
		V_{BOR2}	3.24	3.29	3.35	
		V_{BOR3}	3.66	3.72	3.81	
		V_{BOR4}	4.07	4.15	4.26	
		V_{BOR5}	4.45	4.58	4.71	
		V_{BOR6}	4.87	4.97	5.29	
		V_{BOR7}	5.25	5.44	5.58	
	BOR Detection Level Selection (VDD Falling Edge) (-40°C~105°C)	V_{BOR0}	2.11	2.24	2.31	
		V_{BOR1}	2.55	2.63	2.68	
		V_{BOR2}	2.91	3.05	3.09	
		V_{BOR3}	3.32	3.44	3.51	
		V_{BOR4}	3.68	3.83	3.91	
		V_{BOR5}	4.11	4.23	4.33	
		V_{BOR6}	4.51	4.61	4.71	
		V_{BOR7}	4.79	5.02	5.12	
$V_{BORhyst}$	BOR Hysteresis	-	150	-	400	mV
t_{BORRST}(2)	Effective Time	-	-	10	-	μs

(1) BOR only monitors VDD.

(2) Design guarantee.

4.2.3 On/Off Reset Characteristics

Table 4-6 On/Off Reset Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$V_{POR/PDR}$ (1)	On/Off reset threshold	Falling edge	1.67	1.92	2.16	V
		Rising edge	1.85	2.08	2.35	V
$V_{PDRhyst}$	PDR hysteresis	-	140	160	170	mV
$t_{RSTTEMPO}$ (2)	Reset time	-	-	2	-	ms

(1) PDR and POR only monitors VDD.

(2) Design guarantee.

4.2.4 Internal Reference Voltage

Table 4-7 Internal Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{REFINT}	Internal Reference Voltage	-40 ~ 105°C	-	0.8	-	V

4.2.5 Operating Current Characteristics

Table 4-8 Operating Current Characteristics

Symbol	Mode	Condition	VDD=5V			Unit
			-40°C	25°C	105°C	
I_{run}	Run Mode	SYSCLK= 48MHz; Enable LSI, and turn off the remaining peripherals; All IOs are configured as high impedance state; To retrieve data from Flash, Flash reads for 2 waiting cycles.	7.35	7.63	7.89	mA
		SYSCLK= 8MHz; Enable LSI, and turn off other peripherals; All IOs are configured to high impedance state; Read the value from Flash, and Flash reads 0 waiting cycles.	1.9	2	3.7	mA
		SYSCLK= 40kHz; All IOs are configured to high impedance state; Enable LSI, and turn off other peripherals; The value is read from Flash, and Flash reads 0 waiting cycles.	0.531	0.656	0.687	mA
I_{Sleep1}	Sleep Mode 1	SYSCLK= 48MHz; AHB/APB is enabled; Turn off the core clock and all peripherals; All IOs are configured to high impedance state; RAM and peripheral data are maintained.	4.48	4.68	5.21	mA

Symbol	Mode	Condition	VDD=5V			Unit
			-40°C	25°C	105°C	
I_{Sleep2}	Sleep Mode 2	SYSCLK= 8MHz; AHB/APB is activated; Turn off the core clock and all peripherals; All IOs are configured to high impedance state; RAM and peripheral data are maintained.	1.59	1.67	1.81	mA
		Wake up time	-	1.63	-	μs
I_{Sleep3}	Sleep Mode 3	SYSCLK=40kHz; AHB/APB is enabled; Turn off the core clock and all peripherals; All IO configurations are set to high impedance state; RAM and peripheral data are maintained.	753	808	938	μA
		Wake up time	-	83	-	μs
I_{Stop}	Stop Mode	All clocks stop, HSI and HSE oscillators are turned off, LSI oscillator is turned on, and all peripherals are turned off; the LDO operates in the normal power consumption mode; All IOs are configured as high-impedance state; Backup register is maintained; CPU, RAM, and peripheral data are maintained.	300.5	353.2	487.8	μA
		Wake up time	-	6.25	-	μs
I_{LPstop}	LowPower Stop Mode	All clocks stop, HSI and HSE oscillators are turned off, LSI oscillator is turned on, and all peripherals are turned off; LDO operates in low power consumption mode, with all peripherals turned off; All IOs are configured to high impedance state; Backup register is maintained; CPU, RAM, and peripheral data are maintained.	5.9	8.83	54.3	μA
		Wake up time	-	57	-	μs

4.2.6 External High-speed HSE Clock Characteristics

Table 4-9 HSE Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{OSC_IN}	Oscillator clock frequency	-	4	-	32	MHz
R_F(1)	Feedback resistor	-	-	1.1	-	MΩ
$T_{stb\ (HSE)}$ (2)	Oscillator start time	$V_{SS} \le V_{IO} \le VDD$	-	0.7	1.8	ms
C	Recommended load capacitance resistance minus the equivalent series capacitance of		-	12	-	pF

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
	crystal oscillator （R_S）					
$I_{DD\ (HSE)}$ (1)	Power consumption of HSE oscillator	VDD=3.3V， CL=12pF	-	400	-	μA

(1) Design guarantee.

(2) $T_{stb\ (HSE)}$ refers to the time from the start of HSE to the output of stable frequency signals.

MCU integrates a HSE negative feedback crystal oscillator circuit inside, and the recommended oscillation circuit outside the chip is shown in the following figure:

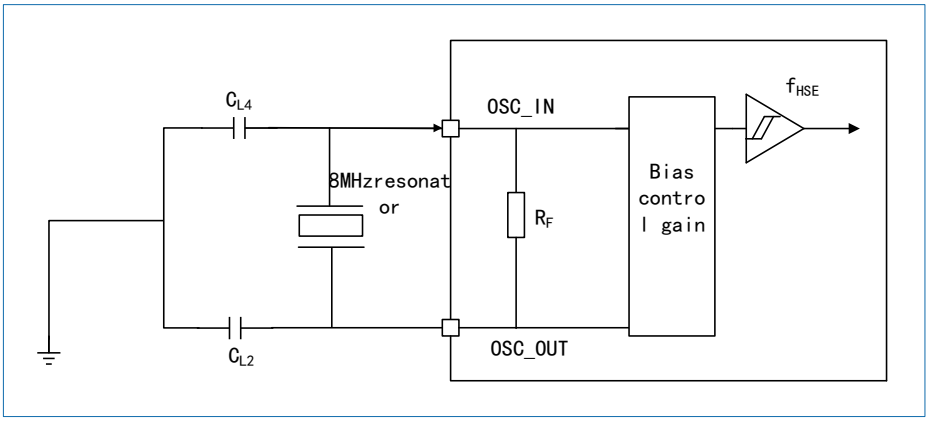

Figure 4-1 HSE negative feedback crystal oscillator

MCU also supports direct input of a clock signal through OSC_IN. The clock signal requirements are as follows.

Table 4-10 External clock Input Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{HSE_ext}	User external clock source frequency	-	4	-	32	MHz
$DuCy_{\ (HSE)}$ (1)	Duty cycle	-	45	-	55	%

(1) Design guarantee.

4.2.7 Internal High-speed HSI Clock Characteristics

Table 4-11 HSI Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{HSI}(1)	Clock frequency	-	-	48	-	MHz
$DuCy_{\ (HSI)}$ (1)	Duty cycle	-	45	50	55	%
$ACC_{\ (HSI)}$	Oscillator accuracy	After the user calibrates the RCC_CR register	-1	-	1	%
		Factory calibration T_A= -40 ~	-1.3	-	1.0	

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
		+105°C				
$T_{stb\ (HSI)}$ (1)	Oscillator start time	$V_{SS} \le V_{IN} \le VDD$	-	8	11	μs
$I_{DD\ (HSI)}$ (1)	Power consumption of oscillator	48MHz, VDD=5V	-	115	145	μA

(1) Design guarantee.

4.2.8 Internal Low-speed LSI Clock Characteristics

Table 4-12 LSI Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{LSI}	Clock frequency	-	-	40	-	kHz
$T_{su\ (LSI)}$ (1)	Oscillator start time	$V_{SS} \le V_{IN} \le VDD$	-	50	150	μs
$I_{DD\ (LSI)}$ (1)	Power consumption of oscillator	-	-	250	-	nA

(1) Design guarantee.

4.2.9 PLL Characteristics

Table 4-13 PLL Characteristics (1)

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
f_{PLL_IN}	Input clock frequency	2	-	48	MHz
	Input clock duty cycle	45	50	55	%
f_{PLL_OUT}	Output clock frequency	6	-	48	MHz
t_{LOCK}	Phase-locking time	-	60	150	μs

(1) Design guarantee.

4.2.10 Characteristics of Flash Memory

Table 4-14 Characteristics of Flash Memory

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{PROG}	Word Write Time	62	62	102	μs
T_{ERASE}	Page Erase Time	100	100	200	ms
	Chip Erase Time	100	100	200	ms
I_{DDPROG}	Word Write Current	-	-	8	mA

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
$I_{DDERASE}$	Page/Chip Erase Current	-	-	9	mA
I_{DDREAD}	Read Current @ 25MHz	-		3	mA
N_{END}	Erase-Write Endurance	100	-	-	千次
t_{RET}	Data Retention Time	10	-	-	年

4.2.11 IO Input Pin Characteristics

Table 4-15 IO Input Pin Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{IH}	Input High Level	VDD=3.3V	0.65*VDD	-	-	V
V_{IL}	Input Low Level	VDD=3.3V	-	-	0.2*VDD	V
V_{IHhys}	Input High Level	VDD=3.3V	0.65*VDD	-	-	V
V_{ILhys}	Input Low Level	VDD=3.3V	-	-	0.2*VDD	V
V_{hys}	Schmitt Trigger Hysteresis Voltage	VDD=3.3V	-	-	0.2*VDD	mV
I_{lkg}	Input Leakage Current	VDD=3.3V； 0<V_{IO}<3.3V	-	5	-	nA
		VDD=3.3V； V_{IO}=5V	-	5	-	nA
R_{PU}	Pull-up Resistor	V_{IO}=V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down Resistor	V_{IO}=VDD	-	33	-	kΩ
C_{IO}(1)	I/O Pin Capacitance	-	-	-	10	pF

(1) Design guarantee.

4.2.12 IO Output Pin Characteristics

Table 4-16 IO Output Pin Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{OH}	Output High Level	2.4V ≤ VDD ≤5.5 V	0.8*VDD	-	-	V
V_{OL}	Output Low Level	2.4V ≤ VDD ≤5.5 V	-	-	0.2* VDD	V

4.2.13 NRST Reset Pin Characteristics

A pull-up resistor is integrated inside the NRST pin, and the periphery can be connected to any circuit or an external RC circuit.

Table 4-17 NRST Pin Input Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{Noise}	Low level is ignored	-	-	80	ns

4.2.14 TIM Counter Characteristics

Table 4-18 TIM1 Characteristics (1)

Symbol	Condition	Minimum	Maximum	Unit
F_{EXT}	Timer external clock frequency for CH1 to CH3	-	$f_{TIMxCLK}/2$	MHz

(1) Design guarantee, $f_{TIMxCLK}$ = 48MHz。

Table 4-19 TIM2/3 Characteristics (1)

Symbol	Condition	Minimum	Maximum	Unit
F_{EXT}	Timer external clock frequency for CH1 to CH4	-	$f_{TIMxCLK}/2$	MHz

(1) Design guarantee, $f_{TIMxCLK}$ = 48MHz。

4.2.15 ADC Characteristics

Table 4-20 ADC Characteristics

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
VDD	Analog supply voltage when ADC is on	-	2.0	5	5.5	V
V_{REFP}	Positive reference voltage	-	2.0	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	12	24	MHz
f_S (1)	sampling frequency	f_{ADC} = 12MHz	-	0.857	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	Please refer to Table 4-25 for details				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
C_{ADC} (1)	sample-and-hold capacitor	-	-	5	-	pF
Jitter$_{ADC}$	ADC trigger conversion jitter	-	-	1	-	Cycles
t_S (1)	Sampling time	f_{ADC} = 12MHz	1.5	-	239.5	Cycles
t_{CONV} (1)	The total conversion time includes the sampling time	f_{ADC} = 12MHz; 12bit resolution	14	-	252	Cycles

(1) Design guarantee.

(2) The specified values only include the ADC timing. It does not include the delay of register access.
The calculation formula for the maximum input impedance RAIN needs to satisfy:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Among them, the value of N resolution is 12.

The allowable error is less than 1/4 LSB Least Significant Bit, LSB.

Table 4-21 Maximum Input Impedance（f_{ADC} = 12 MHz）

Sampling Period Ts（Cycles）	Sampling Time t_S（μs）	Maximum Input Impedance（kΩ）
1.5	0.125	0.577
7.5	1.6	10.8
13.5	1.125	21.1
28.5	2.375	46.9
41.5	3.458	69.3
55.5	4.625	93.3
71.5	5.958	120.8
239.5	19.958	409.5

Table 4-22 ADC Accuracy

Symbol	Parameter	Test Conditions	Typical Value	Maximum	Unit
ET	Total unadjustable error (1)	VDD=V_{REFP}=5V, f_{ADC} = 12 MHz,	-	13	LSB
EO	Offset error (2)		-	3	
EG	Gain error (3)		-	5	
ED	Differential linear error (4)		-	2	
EL	Integral linear error		-	3	

Symbol	Parameter	Test Conditions	Typical Value	Maximum	Unit
	(5)				

(1) Total non-adjustable error: the maximum deviation between the actual transfer curve and the ideal transfer curve.

(2) Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3) Gain error: The deviation between the last ideal transition and the last actual transition.

(4) Differential linear error: the maximum deviation between the actual step and the ideal step.

(5) Integral linear error: The maximum deviation between any actual transition and the end point correlation line.

Explain：

- ADC accuracy and negative injection current: Avoid injecting negative current on any standard non-robust analog input pin, as this can significantly reduce the accuracy of performing conversions on another analog input pin. It is recommended to add a Schottky diode pin to the standard analog pin that may inject negative current to ground.
- Better ADC performance can be achieved within a limited range of V_{DDA}, frequency, and temperature.
- The data is based on characterization results and has not been tested in production.

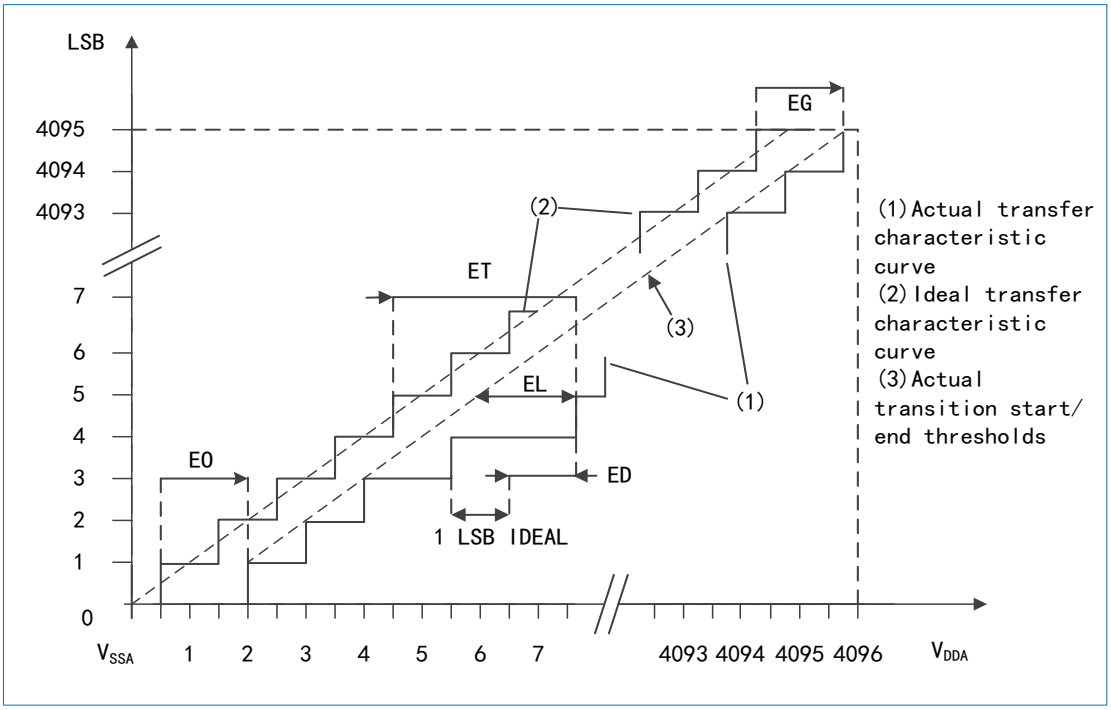

Figure 4-2 ADC Accuracy Characteristics

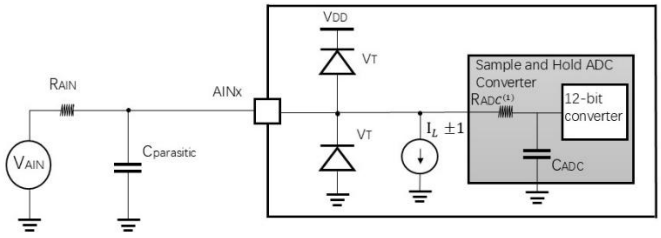

Figure 4-3 Typical Connection Diagram of ADC

(1). The ADC characteristics of RADC and CADC values are shown in Table 4 24.

$C_{parasitic}$ equals PCB capacitance depending on soldering and PCB layout quality plus pad capacitance of approximately 7 pF. A too high tangential value will reduce the conversion accuracy. To compensate for this, f_{ADC} should be minimized.

Recommendations for PCB design for ADC sampling: power decoupling should be carried out according to Figure 5-1. To ensure the accuracy of ADC conversion, it is recommended to use ceramic capacitors with a capacitance of 10 nF and place them as close to the chip as possible.

4.2.16 DAC Voltage Divider Characteristics

Table 4-23 DAC Voltage Divider Characteristics

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
VDD	Analog power supply voltage when DAC is turned on	-	-	5	5.5	V
R_O	Output impedance	DAC buffer is activated	-	7	-	kΩ
I_{OUT}(1)	Output current	DAC buffer is activated	-	-	2	mA

(1) Design guarantee.

4.2.17 Characteristics of Voltage Comparator COMP

Table 4-24 COMP Characteristics

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
VDD	Analog power supply voltage	-	2.2	5	5.5	V
V_{com}	Input common mode	-	0.2	-	5.3	V

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
	voltage					
V_{diff}	Input differential mode voltage	Low-power Low -speed mode	-	-	40	mV
		High-power high-speed mode	-	-	10.5	
V_{hy}	Hysteresis voltage	Gear 1	-	0	-	mV
		Gear 2	-	10	-	
		Gear 3	-	20	-	
I_{OP}	Working current（VDD=5V，static power consumption）	Low-power Low -speed mode	1.405	2.81	3.74	μA
		High-power high-speed mode	22.2	38.55	42.42	
T_{dly}(1)	Output delay（No delay）	High power consumption and high speed mode Rising edge	28.67	42.81	79	ns
		Low power consumption and low speed mode Rising edge	142.3	287.4	753.4	
		High-power high-speed mode Descending edge	30.62	57.8	72.13	
		Low-power low-speed mode Descending edge	206.5	597.2	849.8	

(1) Design guarantee.

4.2.18 Characteristics of Operational Amplifier OPAMP

Table 4-25 OPAMP Characteristics

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
VDD(1)	Analog power supply voltage	-	2.7	5	5.5	V
V_{OUT}	output voltage	-	0.2	-	VDD_A-0.2	V
CMIR	Input common mode voltage	-	0	-	5.5	V
I_{bias}(2)	Input bias current	-	0.8	1	1.2	μA
I_{load}	Output current	R_L=100Ω，VDD=5V	-	6	-	mA
I_q	Working current	Static mode	-	-	1100	μA
I_l(2)	leakage current	Operational amplifier turned off	-	2.00	170.00	nA
V_{OS}	Input bias voltage	Before calibration	-	±15	-	mV
		After calibration	-	±2.5	-	mV

Program	Describe	Condition	Minimum	Typical Value	Maximum	Unit
CMRR(2)	Common mode rejection ratio	-	51	-	145	dB
PSRR(2)	Power supply rejection ratio	-	41	70	109.4	dB
UGF	unit gain bandwidth	-	-	6	6.4	MHz
SR	Pressure swing rate	(5%-95%) rising	5.213	6.251	8.061	V/μs
		(5%-95%) falling	5.278	6.571	8.679	
ϕ	Phase margin	-	47.09	70.93	84.58	Deg
PGA gain	PGA gain	Gear 1	-	1	-	times
		Gear 2	-	2	-	
		Gear 3	-	5	-	
		Gear 4	-	8	-	
		Gear 5	-	10	-	
		Gear 6	-	14	-	
		Gear 7	-	16	-	
		Gear 8	-	20	-	

(1) Please ensure that the operational voltage of the operational amplifier is between 2.7V and 5.5V, and that the operational voltage of other peripherals can be lower than 2.7V;

(2) Design guarantee.

4.2.19 Dynamic Electrical Characteristics of Three-phase Gate Driver

Table 4-26 Dynamic Electrical Characteristics of Three-phase Gate Driver（1）

Parameter		Minimum	Typical Value	Maximum	Unit
Opening delay of the upper tube	T_{ONH}	-	260	450	ns
Upper tube shutdown delay	T_{OFFH}	-	50	200	ns
Opening delay of lower tube	T_{ONL}	-	260	450	ns
Lower tube shutdown delay	T_{OFFL}	-	50	200	ns
Dead Zone Time	DT	-	250	350	ns
delay matching time	MT	-	10	50	ns
Opening up the rise time	T_R	-	20	50	ns
Turn off the falling time	T_F	-	20	30	ns

(1) Test conditions: VIN=24.0V, load capacitance C_L =1000pF, ambient temperature T_A=25℃.

4.2.20 Electrical Characteristics of Three-phase Gate Driver

Table 4-27 Electrical Characteristics of Three-phase Gate Driver

Parameter		Test conditions	Minimum	Typical Value	Maximum	Unit
Working current						
VIN quiescent current	I_{VIN_OFF}	HIN, LIN suspended	-	500	800	uA
	I_{VIN_ON}	HIN, LIN is “1”	-	500	800	uA
Leakage current	I_{LK}	V_B=V_S=60V	-	0.1	-	uA
PWM logic input characteristics						
Logical high voltage	V_{INH}	-	2.0	-	5.0	V
Logic low voltage	V_{INL}	-	0	-	0.8	V
Pull down resistor	R_{PD}	-	-	140	200	kΩ
Protection features						
VBS UVLO rising protection threshold	V_{BSUV_R}	-	-	3.60	-	V
VBS UVLO drop protection threshold	V_{BSUV_F}	-	-	3.30	-	V
VBS UVLO hysteresis	V_{BSUV_H}	-	-	300	-	mV
VCC UVLO rise protection threshold	V_{CCUV_R}	-	-	3.60	-	V
VCC UVLO drop protection threshold	V_{CCUV_F}	-	-	3.30	-	V
VCC UVLO hysteresis	V_{CCUV_H}	-	-	300	-	mV
Output drive capability						
Low side/high side upper tube output voltage	V_{OHL}	I_O=20mA	-	95	-	mV
Low side/high side lower tube output voltage	V_{OLL}	I_O=20mA	-	35	-	mV
Low side/high side upper tube output peak current	I_{OHL}	V_O=0, V_{IN}=5V	-	1.5	-	A
Low side/high side Lower tube absorption peak current	I_{OLL}	V_O=15V, V_{IN}=0V	-	1.8	-	A
When the HIN signal is transmitted normally to the HO, a negative VS voltage is allowed	V_{SN}	V_{BS}=12V	-	-10.0	-	V

4.2.21 LDO Output Characteristics

Table 4-28 LDO Output Characteristics

Parameter		Test Conditions	Minimum	Typical Value	Maximum	Unit
Gate output voltage	V_G	-	-	13.0	-	V
VCC output voltage	VCC	VIN=24V, external NPN 8050	-	12.0	-	V
5V LDO output voltage	V_{LDO5}	-	4.80	4.95	5.10	V
5V LDO output current	I_{LDO5}	-	-	50	-	mA

5 Typical Circuit

5.1 Power Supply

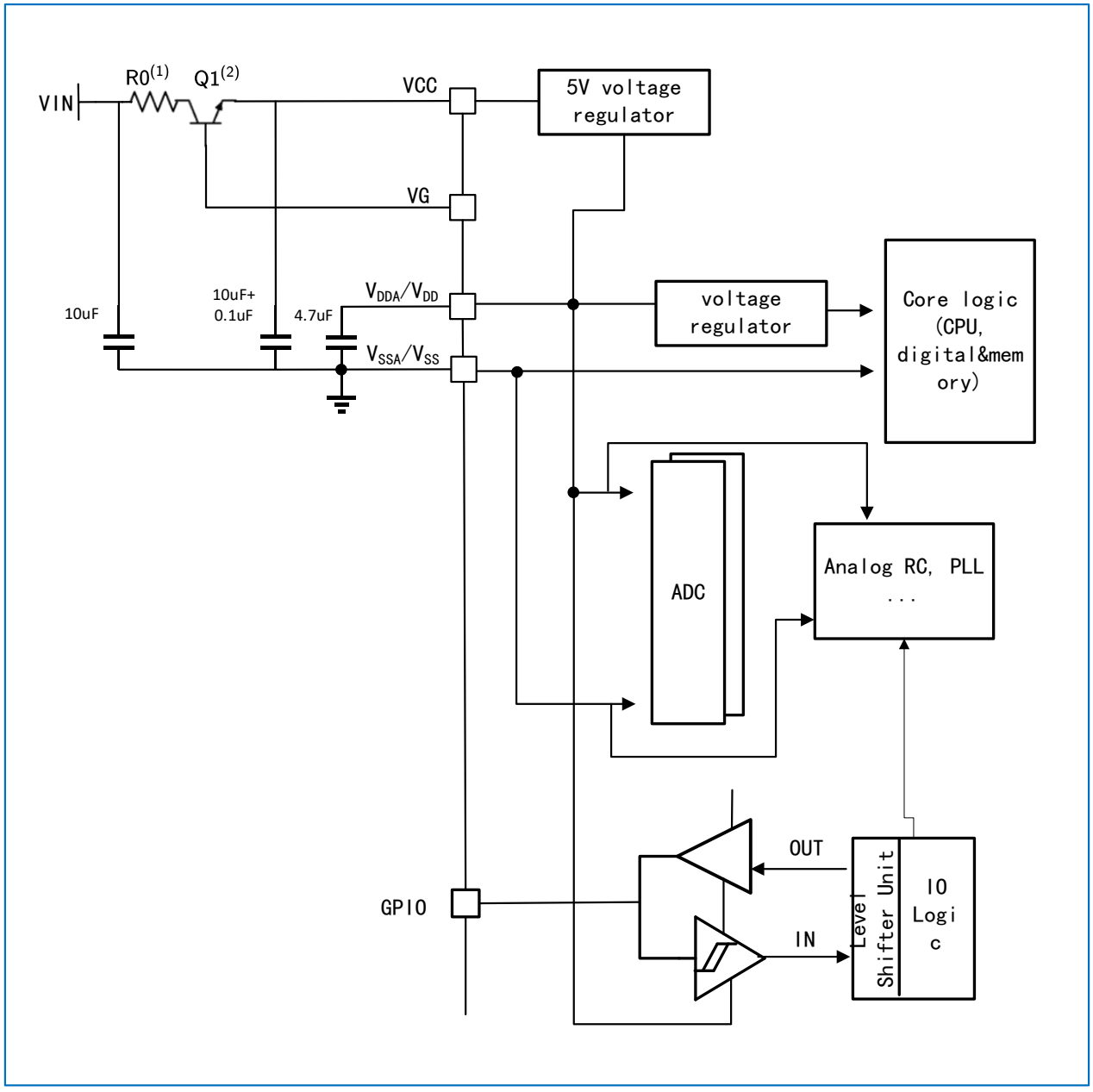

Figure 5-1 Power Diagram

(1). When VIN is greater than 12V, the heat dissipation of Q1 can be optimized by adjusting the resistance of R0.

(2). When VIN≤12V, VIN and VCC can be directly short-circuited, and Q1 and R0 may not be required. When VIN＞12V, it is recommended to retain Q1 to improve power stability.

(3). When the power supply voltage is within 30V, the reference circuit in Figure 5-1 can be used. If the power supply voltage is above 30V, an additional 12V power supply is required to supply VCC.

6 Pin Definition

This series of chips defines the WQFN6x6-48 package, and this chapter introduces the pin definitions for each package.

6.1 WQFN6x6-48 Package

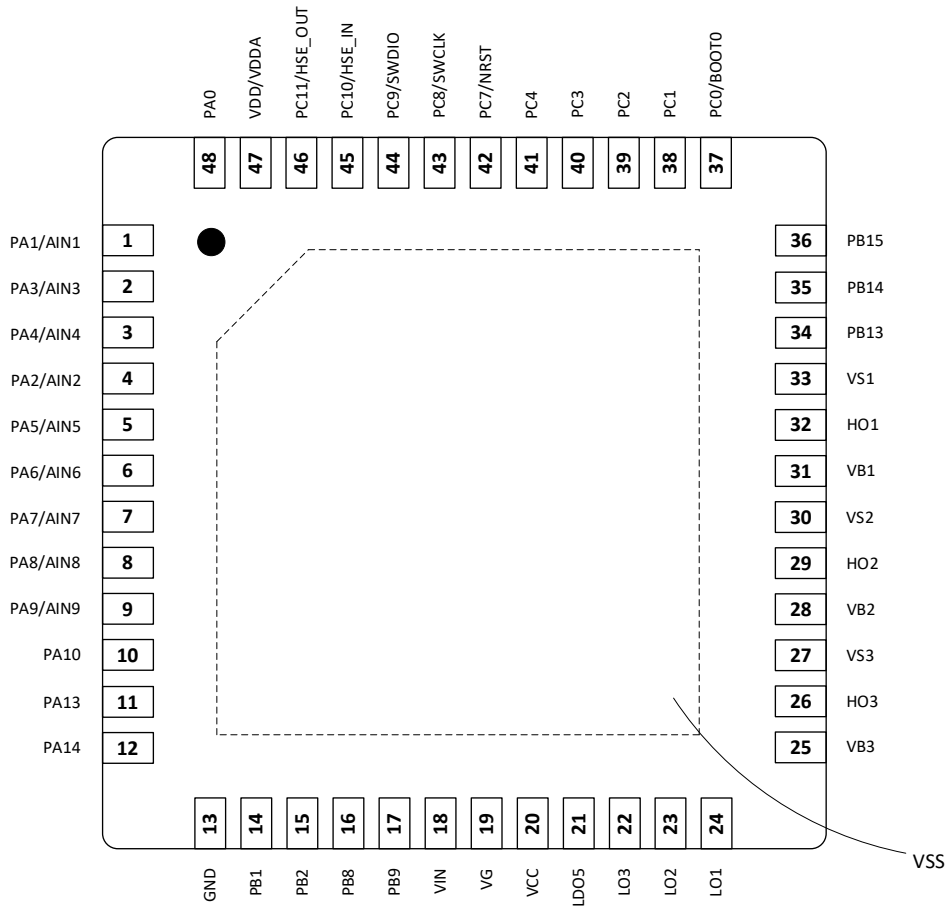

Figure 6-1 Pin Diagram

6.2 Definition of Pins for Each package

Table 6-1 Definition of Pins for Each Package

WQFN6X6-48	Pin Name (Default Function After Reset)	Pin Type (1)	Support 5V Tolerance	Pin Multiplexing Function	Pin Additional Function
1	PA1	I/O	FT	-	ADC_IN1 EXTIN1
2	PA3	I/O	FT	COMP3_OUT	ADC_IN3 OPA2_INN1 EXTIN3
3	PA4	I/O	FT	COMP1_OUT	CKI_1

WQFN6X6-48	Pin Name (Default Function After Reset)	Pin Type (1)	Support 5V Tolerance	Pin Multiplexing Function	Pin Additional Function
					ADC_IN4 EXTIN4
4	PA2	I/O	FT	TIM3_CH1 COMP4_OUT	ADC_IN2 OPA2_OUT1 EXTIN2
5	PA5	I/O	FT	COMP2_OUT TRACE_TX	ADC_IN5 DAC1_OUT EXTIN5
6	PA6	I/O	FT	RCC_MCO	ADC_IN6 COMP1_INP1 EXTIN6
7	PA7	I/O	FT	-	ADC_IN7 OPA1_OUT1 COMP2_INP1 EXTIN7
8	PA8	I/O	FT	RCC_MCO	ADC_IN8 OPA1_INN1 COMP3_INP1 EXTIN8
9	PA9	I/O	FT	-	ADC_IN9 COMP4_INP1 OPA1_INP2 OPA2_INP2 EXTIN9
10	PA10	I/O	FT	-	COMP1_INN0 COMP2_INN0 COMP3_INN0 COMP4_INN0 OPA3_INP1 EXTIN10
11	PA13	I/O	FT	-	OPA1_INP1 OPA2_INP1 EXTIN13
12	PA14	I/O	FT	-	OPA1_PGA_N OPA2_PGA_N COMP1_INP0 COMP2_INP0 COMP3_INP0 COMP4_INP0 OPA3_INP0 EXTIN14
13	GND	S	-	VSS/VSSA	
14	PB1	I/O	FT	-	OPA1_INP0 OPA2_INP0

WQFN6X6-48	Pin Name (Default Function After Reset)	Pin Type (1)	Support 5V Tolerance	Pin Multiplexing Function	Pin Additional Function
					EXTIN1
15	PB2	I/O	FT	TIM1_CH3N TIM1_CH1 TIM1_CH1N	EXTIN2
16	PB8	I/O	FT	TIM1_ETR	EXTIN8
17	PB9	I/O	FT	TIM1_BKIN	EXTIN9
18	VIN	S	-	Chip power supply and LDO5 power input pin	
19	VG	S	-	External NPN base connection pin	
20	VCC	S	-	12V LDO output pin, connected to the emitter of an external NPN transistor	
21	LDO5	S	-	5V LDO output pin	
22	LO3	O	-	Low-side gate driver output of channel 3	
23	LO2	O	-	Low-side gate driver output of channel 2	
24	LO1	O	-	Low-side gate driver output of channel 1	
25	VB3	S	-	Channel 3 high side floating power supply	
26	HO3	O	-	High-side gate driver output for channel 3	
27	VS3	S	-	Channel 3 high side floating ground	
28	VB2	S	-	Channel 2 high side floating power supply	
29	HO2	O	-	High-side gate driver output for channel 2	
30	VS2	S	-	Channel 2 high side floating ground	
31	VB1	S	-	Channel 1 high side floating power supply	
32	HO1	O	-	High-side gate driver output for channel 1	
33	VS1	S	-	Channel 1 high side floating ground	
34	PB13	I/O	FT	TIM1_CH1N TIM1_CH3N SPI_MISO UART1_RX/UART1_TX	EXTIN13
35	PB14	I/O	FT	TIM1_CH2N SPI_MOSI UART1_TX/UART1_RX	EXTIN14
36	PB15	I/O	FT	TIM1_CH3N TIM1_CH1N I2C_SDA UART1_DE	EXTIN15
37	PC0/BOOT0（PC0）	I/O	FT	TIM1_ETR ADC_EXT_TRIG TIM2_CH4	EXTIN0
38	PC1	I/O	FT	TIM2_CH3	EXTIN1

WQFN6X6-48	Pin Name (Default Function After Reset)	Pin Type (1)	Support 5V Tolerance	Pin Multiplexing Function	Pin Additional Function
				SPI_CLK	
39	PC2	I/O	FT	TIM2_CH2 TIM3_CH3 SPI_CS	EXTIN2
40	PC3	I/O	FT	TIM2_CH1 TIM3_CH2 SPI_MISO	EXTIN3
41	PC4	I/O	FT	TIM3_CH1 SPI_MOSI TRACE_TX	CKI_3 OPA3_INP2 EXTIN4
42	PC7/NRST (PC7)	I/O	FT	TIM3_CH4	NRST EXTIN7
43	PC8/SWCLK (SWCLK)	I/O	FT	CM0_SWCLK UART1_TX/UART1_RX ADC_EXT_TRIG	COMP1_INN1 EXTIN8
44	PC9/SWDIO (SWDIO)	I/O	FT	CM0_SWDIO UART1_RX/UART1_TX ADC_EXT_TRIG	COMP2_INN1 EXTIN9
45	PC10/HSE_IN (PC10)	I/O	-	-	HSE_IN COMP3_INN1 OPA3_INN1 EXTIN10
46	PC11/HSE_OUT (PC11)	I/O	-	-	HSE_OUT COMP4_INN1 OPA3_OUT2 EXTIN11
47	VDD/VDDA	S	-	Digital/analog power supply	
48	PA0	I/O	FT	-	CKI_4 ADC_IN0 EXTIN0

(1). I represents input, O represents output, I/O represents input/output, and S represents power supply.

Explain：

- Unless otherwise specified, all I/O are set to analog input during and after reset.
- For pin multiplexing functions, please refer to the "Pin Multiplexing AF Function Table".

6.3 Pin Multiplexing AF Function Table

Table 6-2 Pin Multiplexing AF Function Table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC8	SWCLK	ADC_EXT_TRI	-	-	-	-	UART1_TX	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		G						
PC9	SWDIO	ADC_EXT_TRIG	-	-	-	-	UART1_RX	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PA0-AIN0	-	-	-	-	-	-	-	-
PA1-AIN1	-	-	-	-	-	-	-	-
PA2-AIN2	COMP4_OUT	-	-	-	-	TIM3_CH1	-	-
PA3-AIN3	COMP3_OUT	-	-	-	-	-	-	-
PA4-AIN4	COMP1_OUT	-	-	-	-	-	-	-
PA5-AIN5	COMP2_OUT	-	-	-	-	-	TRACE_TX	-
PA6-AIN6	RCC_MCO	-	-	-	-	-	-	-
PA7-AIN7	-	-	-	-	-	-	-	-
PA8-AIN8	RCC_MCO	-	-	-	-	-	-	-
PA9-AIN9	-	-	-	-	-	-	-	-
PA10	-	-	-	-	-	-	-	-
PA13	-	-	-	-	-	-	-	-
PA14	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-
PB2	-	-	TIM1_CH3N	TIM1_CH1	TIM1_CH1N	-	-	-
PB8	-	-	TIM1_ETR	-	-	-	-	-
PB9	-	-	TIM1_BKIN	-	-	-	-	-
PB13	-	-	TIM1_CH3N	TIM1_CH1N	-	-	UART1_RX	SPI_MISO

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB14	-	-	TIM1_CH2N	TIM1_CH2N	-	-	UART1_TX	SPI_MOSI
PB15	-	-	TIM1_CH1N	TIM1_CH3N	-	-	UART1_DE	I2C_SDA
PC0	-	ADC_EXT_TRIG	TIM1_ETR	-	TIM2_CH4	-	-	-
PC1	-	-	-	-	TIM2_CH3	-	-	SPI_CLK
PC2	-	-	-	-	TIM2_CH2	TIM3_CH3	-	SPI_CS
PC3	-	-	-	-	TIM2_CH1	TIM3_CH2	-	SPI_MISO
PC4	-	-	-	-	-	TIM3_CH1	TRACE_TX	SPI_MOSI
PC7-NRST	-	-	-	-	-	TIM3_CH4	-	-

7 Packaging Parameters

7.1 Package Size

7.1.1 WQFN6x6-48 Package

WQFN6x6-48 is 6 mm x 6 mm, with a 0.4 mm pitch.

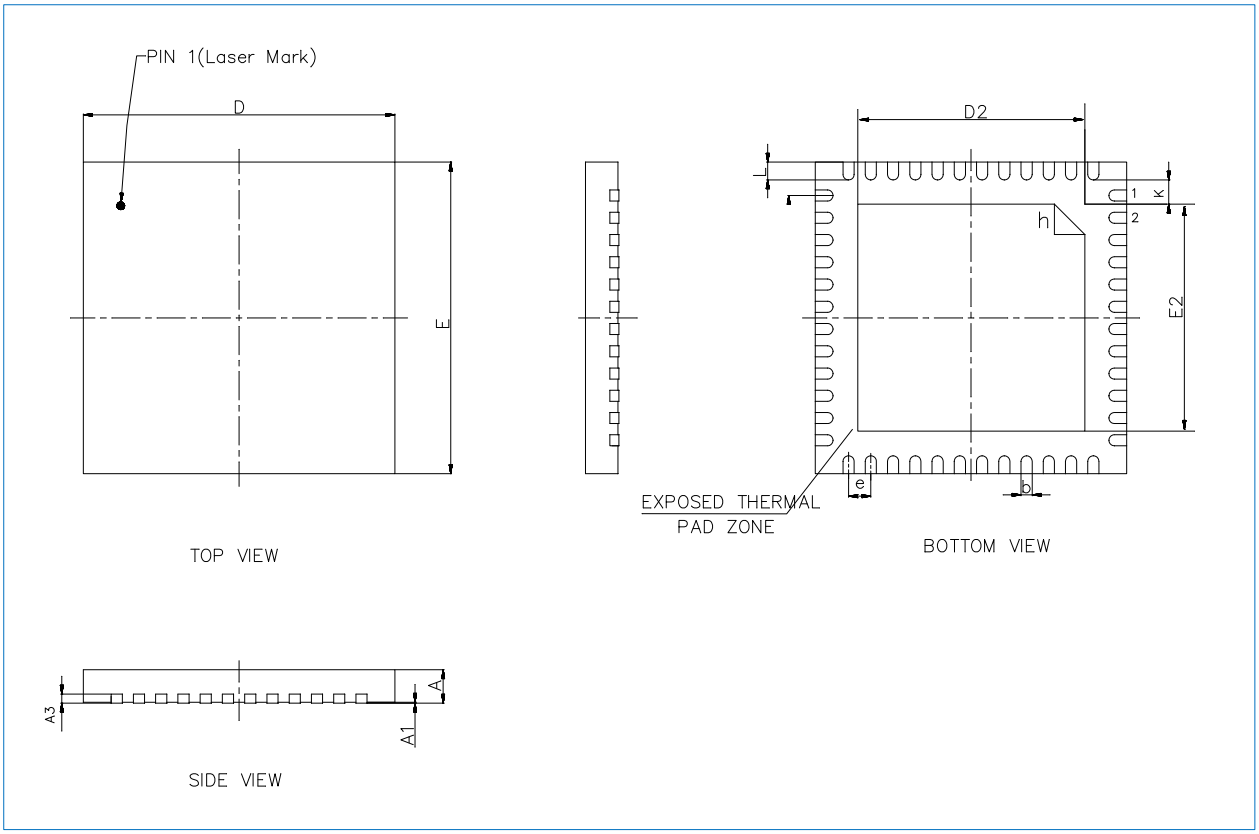

Figure 7-1 WQFN6x6-48 Package Size

Table 7-1 WQFN6x6-48 Package Size Parameter

Symbol	Minimum(mm)	Typical Value(mm)	Maximum(mm)
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF		
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.15	4.20	4.25
E2	4.15	4.20	4.25
b	0.175	0.20	0.225
L	0.375	0.40	0.425

Symbol	Minimum(mm)	Typical Value(mm)	Maximum(mm)
h		0.35	
e		0.40BSC	
K	0.475	0.50	0.525

8 Ordering Information

8.1 Order Information

Table 8-1 Product Ordering Information

Package	Specific Model	Packaging	Top Marking
WQFN6x6-48	PM20025G-08	Disc/Tape	PM20025G 08QW YMDNN

Product code : PM20025G , Voltage/Package code : 08QW

Y : Year code M : Month code D : Day code NN: Serial Number

9 Abbreviation

Abbreviation	Full Name	Chinese Description
ADC	Analog-to-Digital Converter	模拟数字转换器
AHB	Advanced High-Performance Bus	高级高性能总线
APB	Advanced Peripheral Bus	外围总线
AWU	Auto-Wakeup	自动唤醒
CSS	Clock Security System	时钟安全系统
CTS	Clear to Send	清除发送
DMA	Direct Memory Access	直接存储器访问
EXTI	Extended Interrupts and Events Controller	中断和事件控制器
GPIO	General Purpose Input Output	通用输入输出
HSE	High Speed External（Clock Signal）	高速外部（时钟信号）
I2C	Inter-Integrated Circuit	I2C 总线
I2S	Inter-IC Sound	I2S 总线
IWDG	Independent Watchdog	独立看门狗
LSI	Low-Speed Internal（Clock Signal）	低速内部（时钟信号）
MCU	Microcontroller Unit	微控制单元
MSPS	Million Samples Per Second	每秒百万次采样
NVIC	Nested Vectored Interrupt Controller	嵌套矢量中断控制器
PDR	Power-Down Reset	掉电复位
PGA	Programmable Gain Amplifier	可编程的增益放大器
PLL	Phase Locked Loop	锁相环
POR	Power-On Reset	上电复位
PPM	Parts per Million	百万分之一
PWM	Pulse Width Modulation	脉宽调制
RCC	Reset and Clock Control	复位时钟控制
RISC	Reduced Instruction Set Computing	精简指令集计算机
RTS	Request to Send	请求发送

Abbreviation	Full Name	Chinese Description
SPI	Serial Peripheral Interface	串行外设接口
SRAM	Static Random Access Memory	静态随机存储器
SWD	Serial Wire Debug	串行线调试
UART	Universal Asynchronous Receiver Transmitter	通用异步收发器
WWDG	Window Watchdog	窗口看门狗

10 Revision Record

Version	Date	Revision Description
0.5.00	2024/11/8	-Initial Released
0.5.01	2025/4/18	-Dual Logo , PANJIT & MetaWells
0.5.02	2025/4/19	-To modify metawells Inc. to MetaWells Co., Ltd. -To add watermark
0.5.03	2025/4/25	-Modify operating voltage max. rating from 50V to 36V -Translate the pictures from Chinese to English -To add watermark
0.5.04	2025/4/29	-To remove watermark

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