# PJ85775

## ±0.5°C Digital Temperature Sensor with Digital Interface In a SOP8/MSOP-8 Package

## GENERAL DESCRIPTION

The PJ85775 is a digital temperature sensor with ±0.5 °C accuracy. Temperature data can be read out directly via digital interface (compatible with SMBus, I²C or 2-wire) by MCU, Bluetooth Chip or SoC chip.

PJ85775 supports I²C communication with speed up to 400 kHz. Each chip is specially calibrated for ±0.5 °C (Max.) accuracy over 0 °C to 50 °C range in factory before shipment to customers. There is no need for re-calibration anymore for ±0.5 °C accuracy.

It includes a high precision band-gap circuit, a 12-bit analog to digital converter that can offer 0.0625 °C resolution, a calibration unit with non-volatile memory, and a digital interface block.

It includes a band-gap circuit, an Analog to Digital converter, a calibration unit with non-volatile memory and a digital interface block.

It has ALERT logic output pin with open drain structure, which is selectable for active low or high by programming. ALERT response is compatible with SMBus ALERT Response Address (ARA).

PJ85775 can be used as standalone thermostat.

Available Package : SOP-8 and MSOP-8.

## FEATURES

- Operation Voltage : 1.75 V to 5.5 V
- Average Quiescent Current : 3.0 uA(Typ.) at 1.0 con/s
- Standby Current : 1.0 uA (Typ.)
- Temperature Accuracy without calibration :
  - ±0.5 °C from 0 °C to 50 °C
  - ±1.0 °C from -20 °C to 85 °C
  - ±1.5 °C from -40 °C to 125 °C
- 12 bit ADC for 0.0625 °C resolution
- Compatible with SMBus, 2-wire and I²C interface
- Compatible industry LM75 with performance improved
- Programmable Over/Under Temperature
- Programmable Active Low or High for ALERT pin
- Support SMBus ALERT Response Address (ARA)
- Generate 32 different slave address by setup A0, A1, A2 pin
- Temperature Range: -40 °C to 125 °C

## APPLICATIONS

- Smart HVAC System
- Portable Device
- Thermal Management

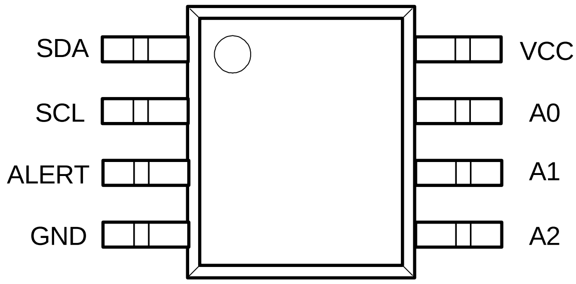
## ORDERING INFORMATION

| Order PN | Accuracy | Green[1] | Package | Marking ID[2] | Packing | MPQ | Operation Temperature |
|---|---|---|---|---|---|---|---|
| PJ85775P_R2 | ±0.5 °C | Halogen free | SOP-8 | PJ85775 PYMDNN | Tape & Reel | 4,000 | -40 °C ~+125 °C |
| PJ85775M_R2 | ±0.5 °C | Halogen free | MSOP-8 | A2 YM DNN | Tape & Reel | 3,000 | -40 °C ~+125 °C |

*(1) Panjit can meet RoHS 2.0/REACH requirement. So most package types Panjit offers only states halogen free, instead of lead free.*

*(2) Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.*

## PIN CONFIGURATION

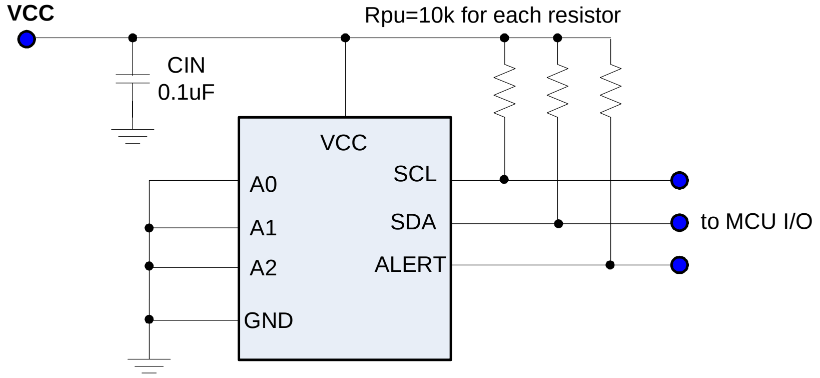



**SOP-8 / MSOP-8 (TOP VIEW)**

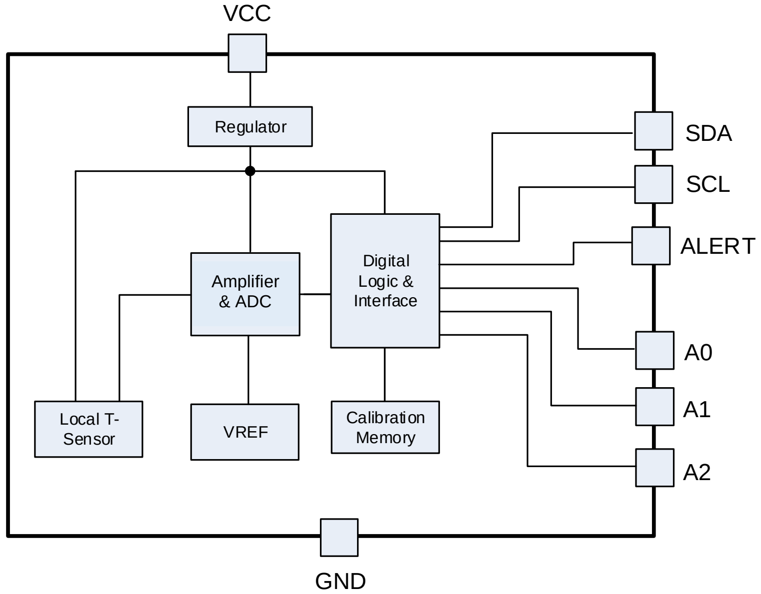
## FUNCTIONAL PIN DESCRIPTION

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NUMBER | NAME | |
| 1 | SDA | Digital interface data input or output pin, need a pull-up resistor to VCC. |
| 2 | SCL | Digital interface clock input pin, need a pull-up resistor to VCC. |
| 3 | ALERT | To Indicate ALERT of over or under Temperature programmed by setting $T_{HIGH}$ / $T_{LOW}$ register, it is open drain output with programmable active low or high. Need a pull-up resistor to VCC in application. |
| 4 | GND | Ground pin. |
| 5 | A2 | Address selection pins, the chip can be defined total 32 different slave address by connecting these pins to GND, VCC, SCL or SDA pin respectively. Do not leave this pins open. See **"Slave Address"** for detail. |
| 6 | A1 | |
| 7 | A0 | |
| 8 | VCC | Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground |

## APPLICATION SCHEMATIC




## FUNCTION BLOCK



## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

| PARAMETER | | MIN | MAX | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ to GND | -0.3 | 7 | V |
| SDA, SCL, A0, A1, A2 Voltage | $V_{SDA}/V_{SCL}/V_{A0}/V_{A1}/V_{A2}$ to GND | -0.3 | 7 | V |
| ALERT Voltage | $V_{ALERT}$ to GND | -0.3 | 7 | V |
| Operating junction temperature range | $T_J$ | -50 | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 | 150 | °C |
| Lead Temperature (Soldering, 10 Seconds) | $T_{LEAD}$ | 260 | | °C |

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## HANDLING RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| ESD(1) | Human Body Model (HBM) ESD stress voltage(2) | -4 | 4 | kV |
| | Charged Device Model (CDM) ESD stress voltage(3), all pins | -1 | 1 | kV |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 1.75 | | 5.5 | V |
| $T_A$ | Operating Ambient temperature | -40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

Test Condition: $C_{IN}$ = 0.1 uF, $V_{CC}$ = 3.3 V, $T_A$ = -40 to 125 °C unless otherwise specified, all limits are 100% test at $T_A$ = 25 °C. (1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | 1.75 | | 5.5 | V |
| $T_{AC}$ | Temperature Accuracy | $T_A$ = 0 to 50 °C | -0.5 | | 0.5 | °C |
| | | $T_A$ = -20 to 85 °C | -1.0 | | 1.0 | °C |
| | | $T_A$ = -40 to 125 °C | -1.5 | | 1.5 | °C |
| $T_{RESOLUTION}$ | Temperature Resolution | | | 0.0625 | | °C |
| $I_{AOC}$ | Average Operating Current | $V_{IN}$ = 3.3 V, 1.0 con/s | | 3.0 | 4.5 | uA |
| $I_{SD}$ | Shutdown Current | STB bit = 1, force SDA/SCL to VCC or GND | | 1.0 | 3.0 | μA |
| $V_{ODL}$ | Open Drain Output Voltage | ALERT pin, sink 5 mA | 0 | | 0.5 | V |
| $I_{ODL}$ | Open Drain Leakage | ALERT pin Leakage | -1.0 | | 1.0 | uA |
| $T_{CON}$ | Conversion time | From active to finish completely | | 30 | | mS |
| **DIGITAL INTERFACE** | | | | | | |
| $C_{IL}$ | Logic Input Capacitance | SDA, SCL pin | | 3.0 | | pF |
| $V_{IH}$ | Logic Input High Voltage | SDA, SCL pin | 0.7x$V_{CC}$ | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Logic Input Low Voltage | SDA, SCL pin | -0.3 | | 0.3x$V_{CC}$ | V |
| $I_{INL}$ | Logic Input Current | SDA, SCL pin | -1.0 | | 1.0 | uA |
| $I_{OLS}$ | Logic Output Sink Current | SDA, ALERT pin forced 0.2 V | | 5.0 | | mA |
| $f_{CLK}$ | SCL frequency | Fast Mode | 1 | | 400 | KHz |
| | | High Speed Mode | 0.001 | | 3 | MHz |
| $t_{LOW}$ | Clock low period time | | 1300 | | | nS |
| $t_{HIGH}$ | Clock high period time | | 600 | | | nS |
| $t_{BUF}$ | Bus free time | Between Stop and Start condition | 1200 | | | nS |
| $t_{HD:STA}$ | Hold time after Start condition | | 600 | | | nS |
| $t_{SU:STA}$ | Repeated Start condition setup time | | 600 | | | nS |
| $t_{SU:STO}$ | Stop condition setup time | | 600 | | | nS |
| $t_{HD:DAT}$ | Data Hold time | | 100 | | | nS |
| $t_{SU:DAT}$ | Data Setup time | | 100 | | | nS |
| $t_F$ | Clock/Data fall time | | | | 300 | nS |
| $t_R$ | Clock/Data rise time | | | | 1000 | nS |

(1) *All devices are 100% production tested at $T_A$ = +25 °C; all specifications over the automotive temperature range is guaranteed by design, not production tested.*

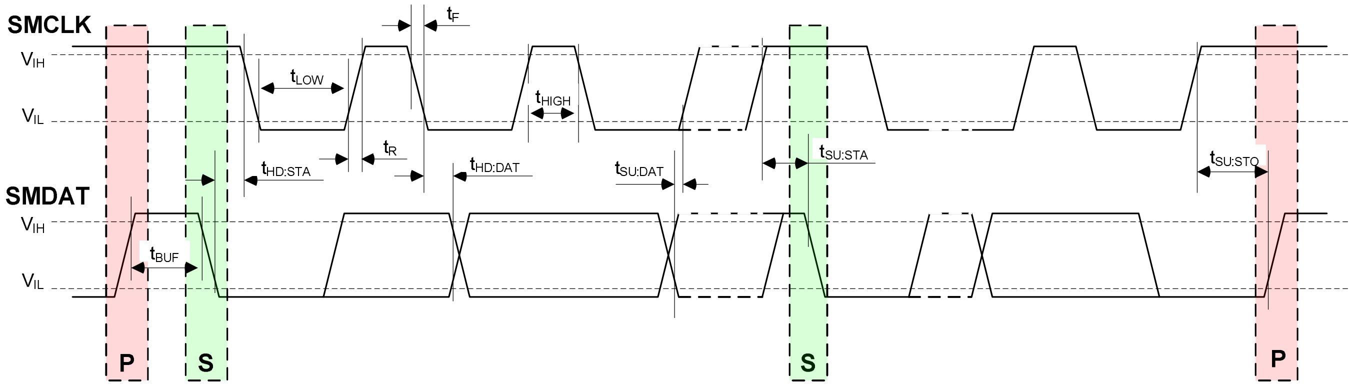



**Figure-1. SMBus / I²C Timing Diagram**

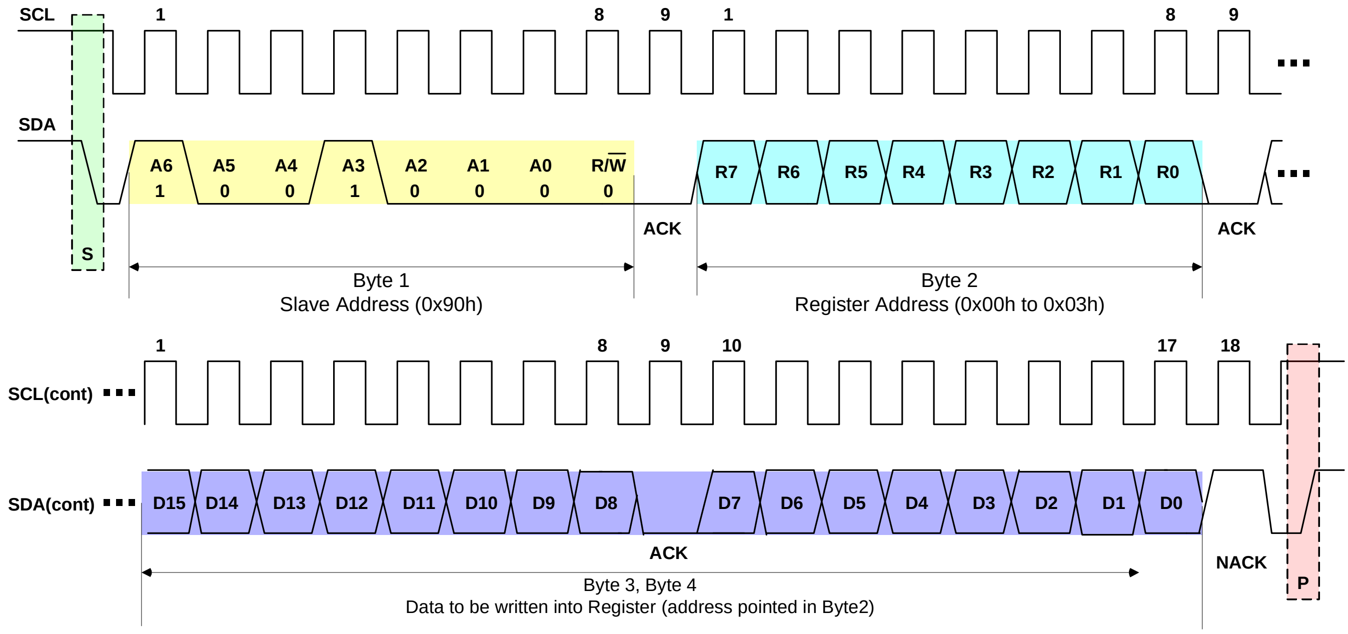



**Figure-2. SMBus / I²C Write Word (2-Bytes) Timing Diagram**

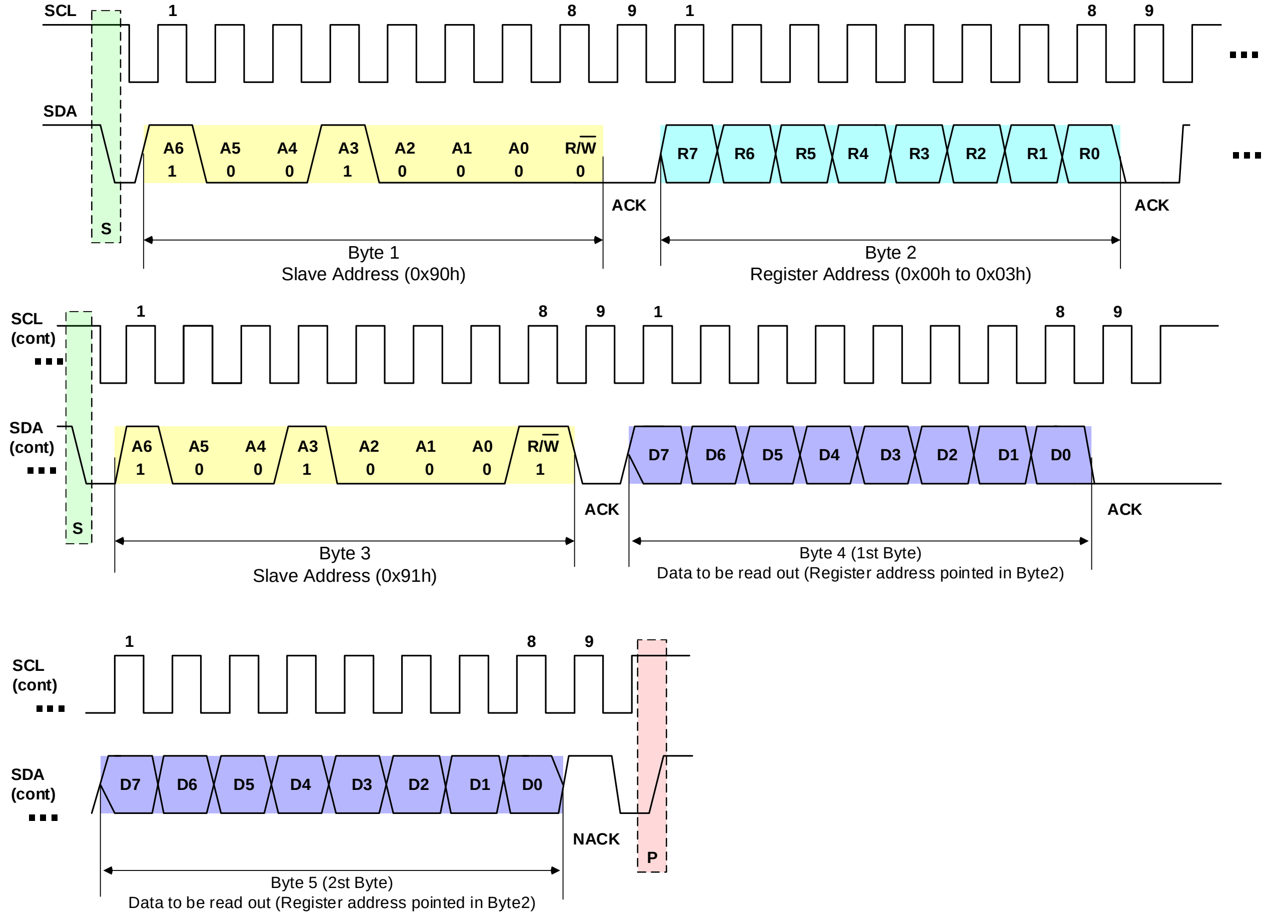



**Figure-3. SMBus / I²C Read Word (2-Bytes) Timing Diagram**

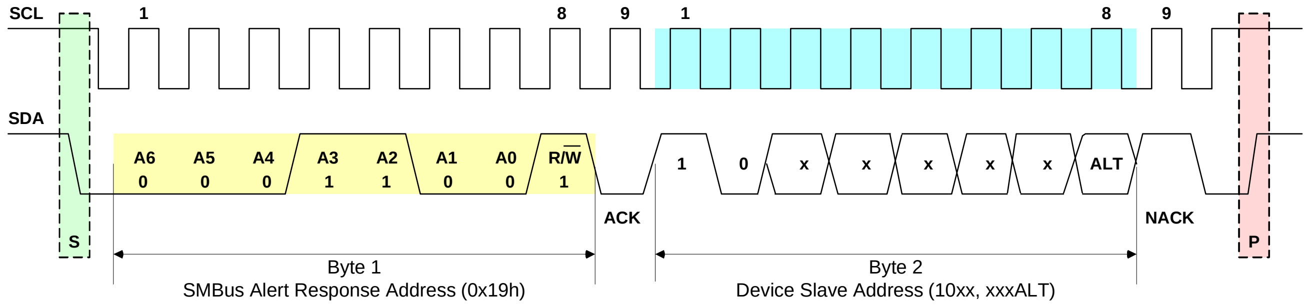



**Figure-4. SMBus ALERT Response Diagram**

## Characteristics ($V_{CC}$ = 3.0 V / 5.0 V)

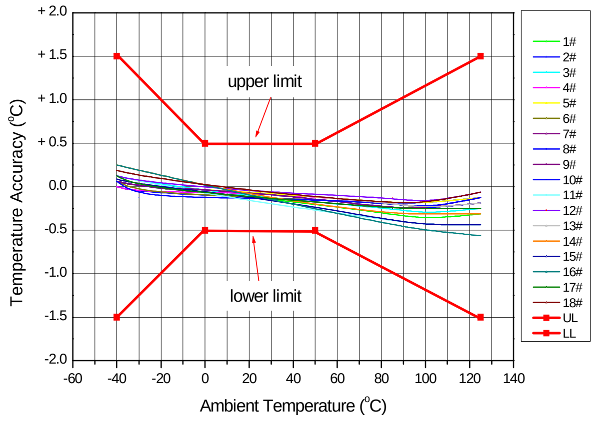



**Figure-5. Temperature Accuracy vs. Temperature**

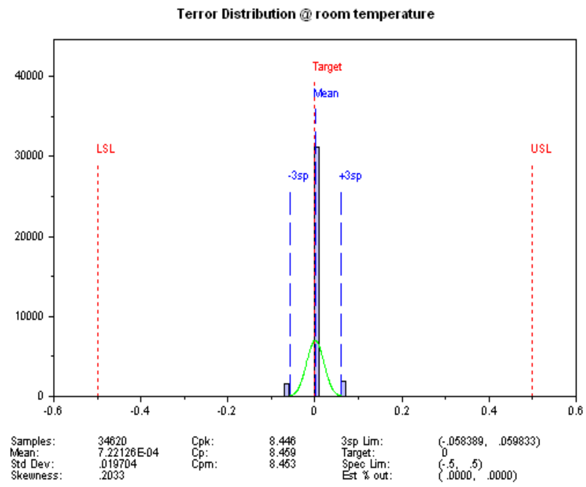



**Figure-8. Temperature Error Distribution**

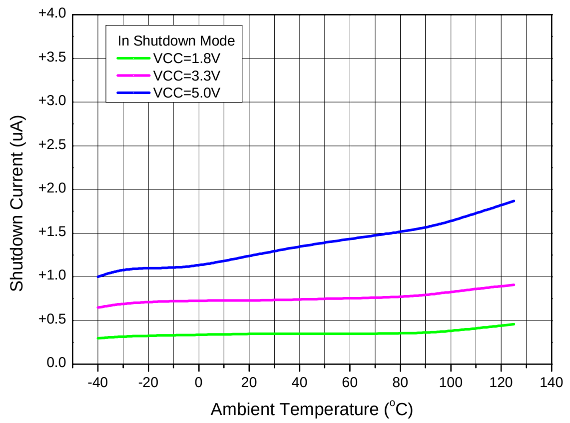



**Figure-6. Shutdown Current vs. Temperature**

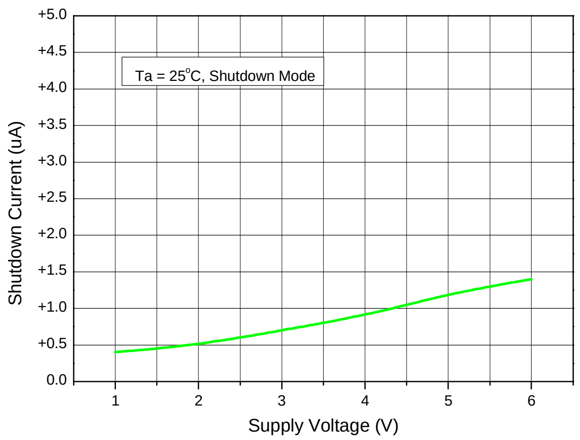



**Figure-7. Shutdown current vs. Supply Voltage**

# FUNCTION DESCRIPTION

## Overview

The chip can sense temperature and convert it into digital data by a 12-bit ADC. Also the chip supports programmable high-/low-limit temperature settings. If the measured temperature meets or exceeds the high-limit temperature, ALERT pin will be asserted (be set low or high, depending on POL bit of configuration register). Once the measured temperature goes below the low-limit temperature (programmable by user), ALERT pin will be released (comparator mode).

## Digital Output of Temperature Data

The temperature measurement data is stored in read only temperature register. The temperature register is in 12-bit binary format (set EM bit as '0') or 13-bit binary format (set EM bit as '1') with 2-Bytes. This 2-Bytes temperature data must be read at the same time in each reading cycle, 1st-Byte is MSB followed by 2nd-Byte, the LSB. The relationship between temperature data in Celsius degree and binary data is shown as below tables.

**Table-1. 12-bit Temperature Data (EM bit = 0)**

| Temperature (°C) | 12-bit Digital Output (HEX) | 12-bit Digital Output (BIN) |
|---|---|---|
| +128.000 | 0x7FF0 | 0 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0) |
| +127.9375 | 0x7FF0 | 0 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0) |
| +100.000 | 0x6400 | 0 1 1 0, 0 1 0 0, 0 0 0 0 (0 0 0 0) |
| +25.000 | 0x1900 | 0 0 0 1, 1 0 0 1, 0 0 0 0 (0 0 0 0) |
| +0.250 | 0x0040 | 0 0 0 0, 0 0 0 0, 0 1 0 0 (0 0 0 0) |
| 0.000 | 0x0000 | 0 0 0 0, 0 0 0 0, 0 0 0 0 (0 0 0 0) |
| -0.0625 | 0xFFF0 | 1 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0) |
| -0.250 | 0xFFC0 | 1 1 1 1, 1 1 1 1, 1 1 0 0 (0 0 0 0) |
| -25.000 | 0xE700 | 1 1 1 0, 0 1 1 1, 0 0 0 0 (0 0 0 0) |

**Table-2. 13-bit Temperature Data (EM bit = 1)**

| Temperature (°C) | 13-bit Digital Output (HEX) | 8-bit Digital Output (BIN) (MSB) 1st Byte | 5-bit Digital Output (BIN) (LSB) 2nd Byte |
|---|---|---|---|
| +150.000 | 0x4B01 | 0 1 0 0, 1 0 1 1 | 0 0 0 0, 0 (0 0 1) |
| +128.000 | 0x4001 | 0 1 0 0, 0 0 0 0 | 0 0 0 0, 0 (0 0 1) |
| +127.9375 | 0x3FF9 | 0 0 1 1, 1 1 1 1 | 1 1 1 1, 1 (0 0 1) |
| +100.000 | 0x3201 | 0 0 1 1, 0 0 1 0 | 0 0 0 0, 0 (0 0 1) |
| +25.000 | 0x0C81 | 0 0 0 0, 1 1 0 0 | 1 0 0 0, 0 (0 0 1) |
| +0.250 | 0x0021 | 0 0 0 0, 0 0 0 0 | 0 0 1 0, 0 (0 0 1) |
| 0.000 | 0x0001 | 0 0 0 0, 0 0 0 0 | 0 0 0 0, 0 (0 0 1) |
| -0.0625 | 0xFFF9 | 1 1 1 1, 1 1 1 1 | 1 1 1 1, 1 (0 0 1) |
| -0.250 | 0xFFE1 | 1 1 1 1, 1 1 1 1 | 1 1 1 0, 0 (0 0 1) |
| -25.000 | 0xF381 | 1 1 1 1, 0 0 1 1 | 1 0 0 0, 0 (0 0 1) |

## Temperature Higher than 128

When temperature is higher than 128 °C, it can be expressed in binary register data by setting EM bit as '1', shown as above Table-2. In extended format, the resolution of AD converter does not change, but '+128' bit is added. For example, 12-bit format for 100°C is 0x6400, in which 0x64 is from 1st Byte, and 0x00 is from 2nd Byte. 13-bit format for 100°C is 0x3201, in which 0x32 is from 1st Byte, and 0x01 is from 2nd Byte. The default for EM bit is '0' after Power-on reset.

## Register Map

The chip has 4 registers assigned address from 0x00 to 0x03, and there are 2 Bytes (1st Byte and 2nd Byte), total 16 bits for each register, shown as below table.

**Table-3. Register Map**

| Register Address | Register Name | Attribution | Default Data | BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00(1) | Temp_MSB (1st Byte) | R/O | N/A | Temp_Data [11:4] | | | | | | | |
| | Temp_LSB (2nd Byte) | R/O | N/A | Temp_Data [3:0] | | | | | | | |
| 0x01 | Config_MSB (1st Byte) | R/W | 0x00 | OS | CR1 | CR0 | F1 | F0 | POL | ALTM | SD |
| | Config_LSB (2nd Byte) | R/W | 0x20 | 0 | 0 | AL | EM | 0 | 0 | 0 | 0 |
| 0x02(1) | Low_Temp_Set_MSB (1st Byte) | R/W | 0x4B | Low_Temp_Setup_Data [11:4] | | | | | | | |
| | Low_Temp_Set_LSB (2nd Byte) | R/W | 0x00 | Low_Temp_Setup_Data [3:0] | | | | | | | |
| 0x03(1) | High_Temp_Set_MSB (1st Byte) | R/W | 0x50 | High_Temp_Setup_Data [11:4] | | | | | | | |
| | High_Temp_Set_LSB (2nd Byte) | R/W | 0x00 | High_Temp_Setup_Data [3:0] | | | | | | | |

*(1) if set EM as '1', Temp data is expressed in 13-bit format, 1st Byte, 8 bits data [12:5] is used as MSB, and 2nd Byte, 5 bits data [4:0] in left justified is used as LSB.*

## Register Description

### Temp_Data, Temperature Data

- Register Address: 0x00
- Register Attribution: Read only
- Default Data: N/A

| BIT (1st Byte) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: Temp_MSB (1st Byte) | Temp_Data[11:4] | | | | | | | |
| Temperature Data (°C) [12-bit] | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 12-bit format | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |
| Temperature Data (°C) [13-bit] | (SIGN) | (128) | (64) | (32) | (16) | (8) | (4) | (2) |
| 13-bit format | (T12) | (T11) | (T10) | (T9) | (T8) | (T7) | (T6) | (T5) |

| BIT (2nd Byte) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: Temp_LSB (2nd Byte) | Temp_Data[3:0] | | | | | | | |
| Temperature Data (°C) [12-bit] | 0.5 | 0.25 | 0.125 | 0.0625 | 0 | 0 | 0 | 0 |
| 12-bit format | T3 | T2 | T1 | T0 | 0 | 0 | 0 | 0 |
| Temperature Data (°C) [13-bit] | (1) | (0.5) | (0.25) | (0.125) | (0.0625) | 0 | 0 | (1) |
| 13-bit format | (T4) | (T3) | (T2) | (T1) | (T0) | (0) | (0) | (1) |

## Config, Configuration Setup register

- Register Address: 0x01
- Register Attribution: Read/Write
- Default Data: 0x00 for 1st Byte, 0x20 for 2nd Byte after POR. If user used only 1-Byte, it is ok to read/write 1-Byte command via digital interface; the only 1st Byte (MSB) will be accessed.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1st Byte | OS | CR1 | CR0 | F1 | F0 | POL | ALTM | SD |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2nd Byte | Reserved | | AL | EM | Reserved | | | |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

- **OS, One shot Conversion bit**
  When the device is in shutdown mode, setting this bit as ‘1’ will trigger a single time temperature conversion. During the conversion, the OS bit reads as ‘0’. The device returns to shutdown mode once it completes the single conversion. This feature is used for reducing power consumption when continuous temperature monitoring is not necessary.

- **CR1, CR0, Conversion Rate Selection bits**
  These 2 bits allow user to setup different conversion rate for temperature. The default is 00 after POR, meaning the conversion rate is 8Hz, i.e. 8 times conversion every second.

| CR1 | CR0 | Conversion Rate / Conversion Time |
|---|---|---|
| 0 | 0 | 8.0Hz / 0.125s (default) |
| 0 | 1 | 4.0Hz / 0.25s |
| 1 | 0 | 1.0Hz / 1.0s |
| 1 | 1 | 0.25Hz / 4.0s |

- **F1, F0, Fault Queue bits**
  These 2 bits are used to setup the number of fault conditions to trigger alert. The default is 00 after POR, which means one time fault. This feature is used to prevent a false alert, which is immune to certain noise in application.

| F1 | F0 | Fault Queue Number |
|---|---|---|
| 0 | 0 | 1 (default) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

- **POL, Alert Output Polarity bit**
  This bit allows user to setup the polarity of ALERT pin for output. The default is 0 after POR, meaning ALERT pin is active low. When POL bit is set as ‘1’, the ALERT pin becomes active high and the state of ALERT pin is inverted.

- **ALTM, Alert Operation Mode bit**
  This bit allows user to select ALERT pin operation mode: Comparator Mode or Interrupt Mode. The default is 0 after POR to select Comparator Mode. For detail information, see ALERT output section.

- **SD, Shutdown bit**
  This bit allows user to shut down the chip and to make the chip enter into standby mode once writing ‘1’. The default value is ‘0’, which sets the chip to be in Normal working mode. During shutdown mode, the temperature data is kept as those of last time, no anymore update, and all function blocks are turned-off except interface. Set this bit as '0' can allow the chip be out of shutdown mode. In shutdown mode, the operation current is about 1.0 uA in typical.

- **EM, Extended Mode bit**
  This bit allows user to select 12-bit (EM = 0) or 13-bit (EM = 1) temperature data. When EM bit is set as '1', the temperature resolution is still 0.0625 °C resolution. However, the expression range is extended from -255 to +255.

- **AL, Alert Status bit**
  The AL bit indicates the Alert status with read-only attribution. In addition, this bit is always read as the inversion of POL bit. When the POL bit equals 0, the AL bit reads as 1 until the measured temperature equals or exceeds Temperature (HIGH) for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below Temperature (LOW) for the programmed number of consecutive faults, when it again reads as 1. Vice versa, when the POL bit is '1', the AL bit reads as 0 until the temperature equals or exceeds Temperature (HIGH). And the AL bit is set as 0 again once the temperature falls below Temperature (LOW). The status of the TM bit does not affect the status of the AL bit.

## Low_Temp_Set, Setup Low Temperature Limitation register

- Register Address: 0x02
- Register Attribution: Read/Write
- Default Data: 0x4B (1st Byte) 0x00 (2nd Byte) after POR

| BIT | BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1st Byte | 12-bit | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |
| | 13-bit | (L12) | (L11) | (L10) | (L9) | (L8) | (L7) | (L6) | (L5) |
| | Default | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 2nd Byte | 12-bit | L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 |
| | 13-bit | (L4) | (L3) | (L2) | (L1) | (L0) | (0) | (0) | (0) |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The high-/low- limit temperature data is determined by High_Temp_Set register [0x03] and Low_Temp_Set register [0x02] with same format as Temp_Data register [0x00], which could be in 12-bit or 13-bit binary format. The chip compares Temp_Data [0x00] register and High_Temp_Set register [0x03]/Low_Temp_Set register [0x02] in each conversion cycle, which will affect ALT pin output. The default value is 0x4B00 with 12-bit binary format, which means 75 °C. For other low-limit temperature data chip, please contact our sales.

## High_Temp_Set, Setup High Temperature Limitation register

- Register Address: 0x03
- Register Attribution: Read/Write
- Default Data: 0x50 (1st Byte) 0x00 (2nd Byte) after POR

| BIT | BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1st Byte | 12-bit | H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |
| | 13-bit | (H12) | (H11) | (H10) | (H9) | (H8) | (H7) | (H6) | (H5) |
| | Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2nd Byte | 12-bit | H3 | H2 | H1 | H0 | 0 | 0 | 0 | 0 |
| | 13-bit | (H4) | (H3) | (H2) | (H1) | (H0) | (0) | (0) | (0) |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The high-/low- limit temperature data is determined by High_Temp_Set register [0x03] and Low_Temp_Set register [0x02] with same format as Temp_Data register [0x00], which could be in 12-bit or 13-bit binary format. The chip compares Temp_Data [0x00] register and High_Temp_Set register [0x03]/Low_Temp_Set register [0x02] in each conversion cycle, which will affect ALT pin output. The default value is 0x5000 with 12-bit binary format, which means 80 °C. For other low-limit temperature data chip, please contact our sales.

## SMBus Digital Interface

### Slave Address

The SMBus or I²C slave address of this device can be configured 32 different addresses by setting [A2], [A1] and [A0] pin. See below table for detail, which permit connecting total 32 devices in one SMBus.

| No. | A2 | A1 | A0 | R/W | Slave Address in Hex [R/W] |
|---|---|---|---|---|---|
| 1 | GND | GND | GND | 1/0 | 0x91/0x90 |
| 2 | GND | GND | VCC | 1/0 | 0x93/0x92 |
| 3 | GND | VCC | GND | 1/0 | 0x95/0x94 |
| 4 | GND | VCC | VCC | 1/0 | 0x97/0x96 |
| 5 | VCC | GND | GND | 1/0 | 0x99/0x98 |
| 6 | VCC | GND | VCC | 1/0 | 0x9B/0x9A |
| 7 | VCC | VCC | GND | 1/0 | 0x9D/0x9C |
| 8 | VCC | VCC | VCC | 1/0 | 0x9F/0x9E |
| 9 | GND | GND | SDA | 1/0 | 0x81/0x80 |
| 10 | GND | GND | SCL | 1/0 | 0x83/0x82 |
| 11 | GND | VCC | SDA | 1/0 | 0x85/0x84 |
| 12 | GND | VCC | SCL | 1/0 | 0x87/0x86 |
| 13 | VCC | GND | SDA | 1/0 | 0x89/0x88 |
| 14 | VCC | GND | SCL | 1/0 | 0x8B/0x8A |
| 15 | VCC | VCC | SDA | 1/0 | 0x8D/0x8C |
| 16 | VCC | VCC | SCL | 1/0 | 0x8F/0x8E |
| 17 | GND | SDA | SDA | 1/0 | 0xA1/0xA0 |
| 18 | GND | SDA | SCL | 1/0 | 0xA3/0xA2 |
| 19 | GND | SCL | SDA | 1/0 | 0xA5/0xA4 |
| 20 | GND | SCL | SCL | 1/0 | 0xA7/0xA6 |
| 21 | VCC | SDA | SDA | 1/0 | 0xA9/0xA8 |
| 22 | VCC | SDA | SCL | 1/0 | 0xAB/0xAA |
| 23 | VCC | SCL | SDA | 1/0 | 0xAD/0xAC |
| 24 | VCC | SCL | SCL | 1/0 | 0xAF/0xAE |
| 25 | GND | SDA | GND | 1/0 | 0xB1/0xB0 |
| 26 | GND | SDA | VCC | 1/0 | 0xB3/0xB2 |
| 27 | GND | SCL | GND | 1/0 | 0xB5/0xB4 |
| 28 | GND | SCL | VCC | 1/0 | 0xB7/0xB6 |
| 29 | VCC | SDA | GND | 1/0 | 0xB9/0xB8 |
| 30 | VCC | SDA | VCC | 1/0 | 0xBB/0xBA |
| 31 | VCC | SCL | GND | 1/0 | 0xBD/0xBC |
| 32 | VCC | SCL | VCC | 1/0 | 0xBF/0xBE |

### Timeout

The chip supports SMBus timeout. If the data (SDA PIN) or clock (SCL PIN) is held low for longer than 30 ms (Typ.), the chip will reset its SMBus protocol and be ready for a new transmission.

## SMBus Protocol

The chip supports four standard SMBus protocols Send Byte, Read Byte, Write Byte and Receive Byte, shown as below tables.

Write Byte

| S | Slave Add | R/W | ACK | Reg Add | ACK | Reg Data | ACK | P |
|---|---|---|---|---|---|---|---|---|
| | 0x80 to 0xBE | 0 | 0 | 0x00 to 0x03 | 0 | XXh | 0 | |

Read Byte

| S | Slave Add | R/W | ACK | Reg Add | ACK | S | Slave Add | R/W | ACK | Reg Data | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0x80 to 0xBE | 0 | 0 | 0x00 to 0x03 | 0 | | 0x80 to 0xBE | 1 | 0 | XXh1 | 1 | |

Send Byte

| S | Slave Add | R/W | ACK | Reg Add | ACK | P |
|---|---|---|---|---|---|---|
| | 0x80 to 0xBE | 0 | 0 | XXh | 0 | |

Receive Byte

| S | Slave Add | R/W | ACK | Reg Add | NACK | P |
|---|---|---|---|---|---|---|
| | 0x80 to 0xBE | 1 | 0 | XXh | 1 | |

Here S means SMBus Start to communication; P, means communication STOP.

Slave Add, means the chip's slave address.

Reg Add, means pointed register address.

Reg Data, means data to be written into register or read from register.

For this chip, each register includes 2 Bytes, so generally reading or writing operation is based on 1 Word (2-Bytes). Also it is permitted to read 1 byte for read/write, and then the 1st byte will be accessed in first.

## Compatible with I$^2$C

The chip is compatible with both SMBus and I$^2$C. The major difference between SMbus and I$^2$C are shown as below. For more information, refer to SMBus specification v2.0 and I$^2$C specification v2.1.

(1). Besides DC specification difference, this chip supports I$^2$C fast mode (400kHz) and standard mode (100kHz), which can cover SMBus maximum frequency 100kHz. For SMBus protocol, the minimum frequency is 10 kHz. There is no such limitation for I$^2$C.

(2). For SMBus protocol, the communication will be reset if holding clock or data low with duration over 30ms (Typ.). There is no timeout for I$^2$C.

(3). ARA (Alert Response Address) general call is only valid interrupt in SMBus, not valid in I$^2$C.

## General Call

The PJ85775 device responds to a two-wire general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the PJ85775 internal registers are reset to power-up values.

### High-Speed (HS) Mode

If the master needs to run at frequencies above 400 kHz in I²C, the master device must issue an HS-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. After the HS-mode master code has been issued, the master transmits a slave address to initiate a data-transfer operation. The bus continues to operate in HS-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the PJ85775 device will return to fast-mode operation. Below is the example for reading operation in high speed mode.

| S | HS-mode code | Slave Add | R/W | ACK | Reg Add | ACK | Sr | Slave Add | R/W | ACK | Reg Data | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0x08 to 0x0F | 0x80 to 0xBE | 0 | 0 | 0x00 to 0x03 | 0 | | 0x80 to 0xBE | 1 | 0 | XXh | 1 | |

## ALERT Output

ALERT pin is output with open drain, which can be set active low or active high by setting POL bit. In addition, this pin is triggered when the measured temperature equals or exceeds the high-limitation temperature setup in the registers of High_Temp_Set. There are two types of ALERT output mode: comparator mode and interrupt mode.

### Comparator mode (ALTM = 0)

Below Figure shows the mechanism of the ALERT output in comparator mode. In this mode, the ALERT pin will becomes active if the monitored temperature equals or exceeds the value setup in High_Temp_Set [0x03] register for a consecutive number of faults according to setup by F1 and F0 bits. The ALERT pin keeps active until the temperature falls below the value setup in Low_Temp_Set [0x02] register.

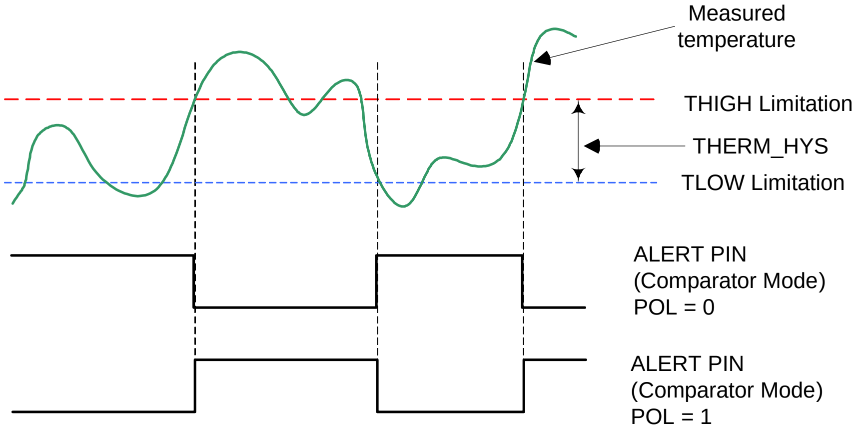



**Figure-9. ALERT pin output in comparator mode**

### Interrupt mode (ALTM = 1)

Below Figure shows the mechanism of the ALERT pin output in interrupt mode. In this mode, the ALERT pin becomes active when the temperature equals or exceeds the value setup in High_Temp_Set [0x03] register for a consecutive number of faults according to setup by F1 and F0 bits. The ALERT pin keeps active until a read operation of any register happens or the chip responds to SMBus Alert Response Address (ARA) successfully. When ALERT pin is cleared, it will become active again only when the temperature falls below the value setup in Low_Temp_Set [0x02] register, and keeps active until being cleared by reading register or responding to SMBus ARA, ALERT pin is also cleared by setting the chip in shutdown mode.

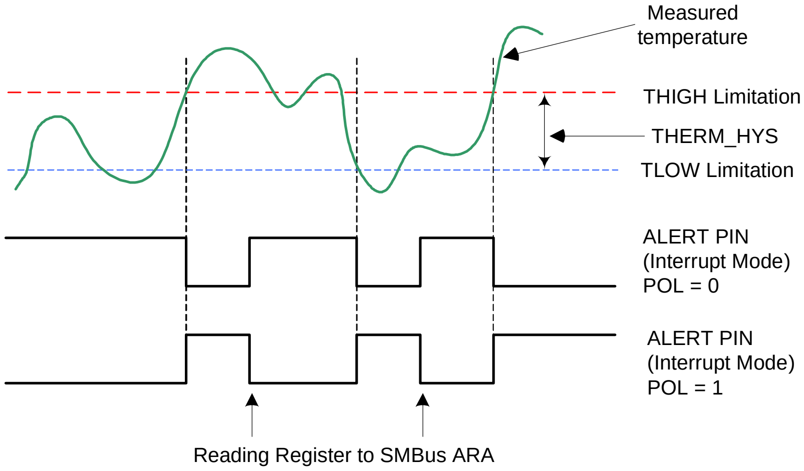



**Figure-10. ALERT pin output in interrupt mode**

## SMBus Alert Response Address (ARA)

The chip supports the SMBus alert function feature. When the chip operates in interrupt mode (ALTM = 1), it can be connected as SMBus alert signal, used as a processer interrupt or as SMBus ALERT. When the master detects that the ALERT pin is asserted, it will send Alert Response Address (ARA) to general address (0001, 1001b). All devices with active interrupts will respond with client address. If the alert pin is active, the device acknowledges the SMBus command by returning the slave address from SDA line. If more devices than one on the bus respond SMBus ARA, arbitration during the slave address portion of SMBus ARA determines which device clears the alert trigger. The device with the highest priority (lowest address) wins the arbitration. If the chip wins the arbitration, ALERT pin is released after completion of SMBus ARA command. If the chip loses the arbitration, it will keep ALERT pin active. See System Management Bus (SMBus) Specification for more detail. Below Figure shows the mechanism of the ALERT output SMBus Alert mode.

| S | Slave Add | R/W | ACK | Reg Add | ACK | P |
|---|---|---|---|---|---|---|
| | 0001,100 | 1 | 0 | 100x,xxxS | 1 | |

Here Reg Add presented the chip real actual address setup by user. S bit indicates if the alert condition is caused by the temperature exceeding T (HIGH) or falling below T (LOW). The S bit is '1' if the temperature is greater than T (HIGH), or '0' if the temperature is less than T (LOW).

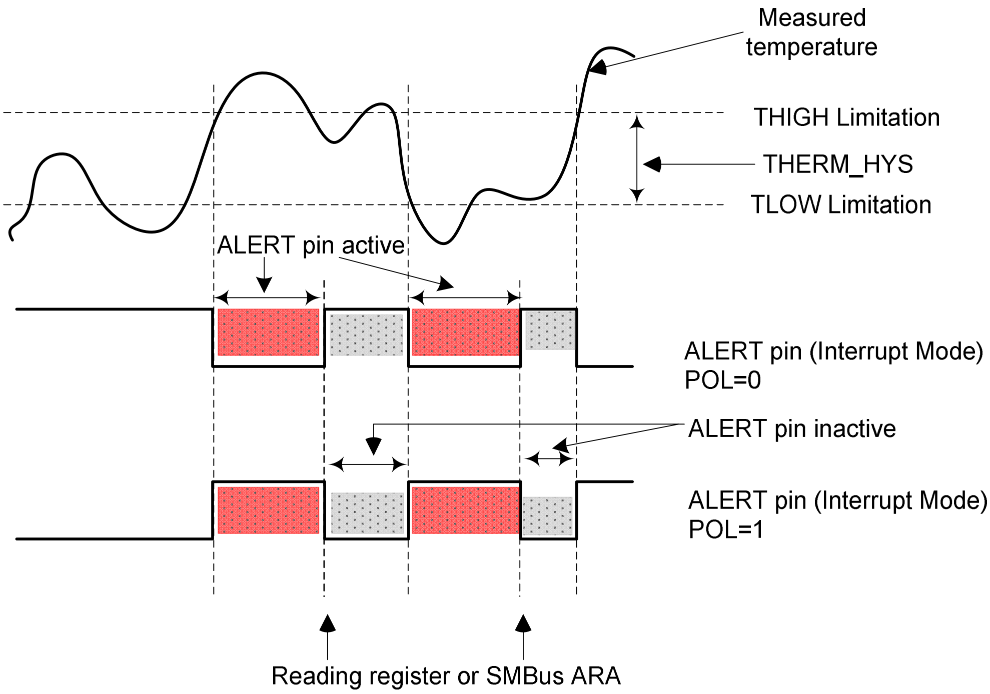



**Figure-11. ALERT pin in SMBus Alert Response (ARA)**

## Applications Information

### How to Improve Temperature Accuracy

The temperature measurement of the chip is based on semiconductor physics principle. Forward voltage of diode is a function of temperature. The formula is shown as below.

$$V_F = \frac{kT}{q}\ln\left(\frac{I_F}{I_S}\right)$$

Here,

*$V_F$ - forward voltage*
*$I_F$ - forward current*
*$I_S$ - reverse saturation current*
*k - Boltzmann constant*
*T - Temperature in K*
*q - Electric charge con*stant

To cover wide temperature range, i.e. -40 °C to 125 °C, a very small voltage variation is corresponding to every degree C temperature change. Panjit has applied many ways to improve measurement accuracy in chip circuits design, such as compensation, trimming etc. In real system design, however, some factors that can increase measurement error need to be considered. Most issues that usually occur are highlighted as below.

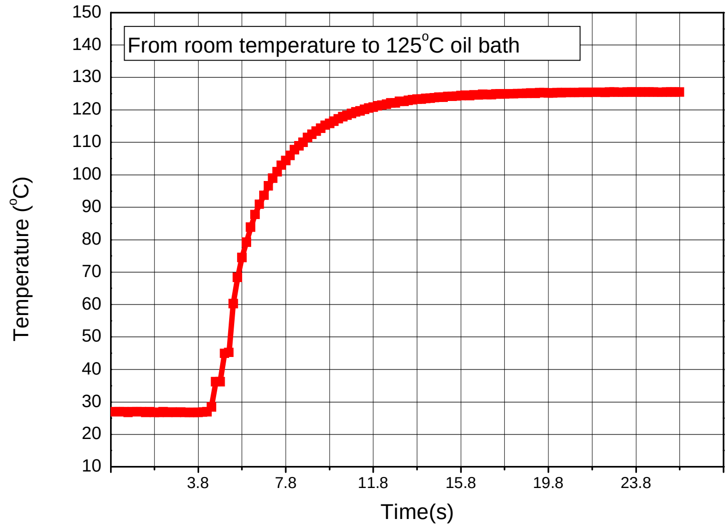
#### Noise between VCC and GND

It is very necessary to place a low ESR ceramic cap ($C_{IN}$) between VCC and GND pin to filter digital noise, although suppression noise circuit has been built inside the chip. This filter cap should be placed as close as possible to the chip. The recommended capacitance is 0.1 uF.

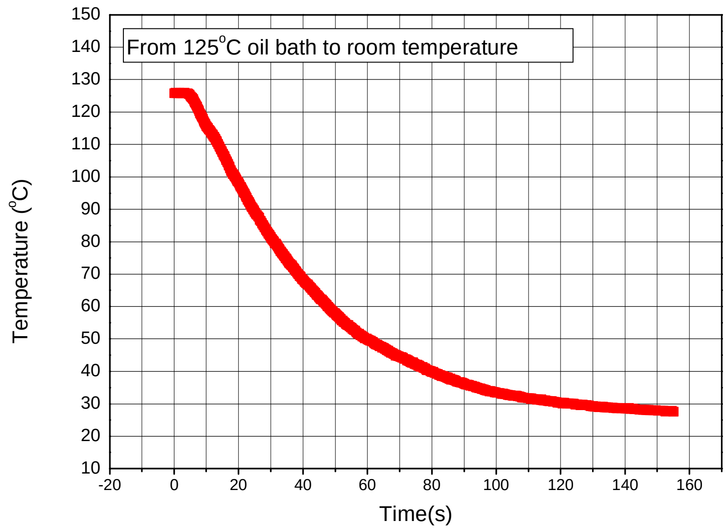
#### Thermal Response Time

It is very necessary to wait enough time for obvious temperature changing of target due to thermal time constant, e.g. food temperature could change from -20 °C to 20 °C when taken out of refrigerator, which could take over ten minutes to reach thermal equilibrium eventually. Enough time is still needed for the target to reach thermal equilibrium, even forcing temperature transient into target object. For this chip, the temperature step response changing from room temperature to oil bath of 125 °C is shown as below. (Based on SOP-8 package)

| Room Temperature | Target Temperature | Change ratio | Delta T | Time (s) |
|---|---|---|---|---|
| 26.8 °C | 125.0 °C | 63% | 61.9 °C | 2.3 |
| | | 80% | 78.5 °C | 3.8 |
| | | 90% | 88.4 °C | 5.6 |
| | | 100% | 98.2 °C | 20.0 |




Vice versa, it will take longer time, about 150 s, when the chip temperature is back to room temperature, once taking the chip out of oil bath of 125 °C. See below plot.




## PCB Layout

Cautions below are important to improve temperature measurement in PCB layout design.

### Device placement

It is better to place the chip away from any thermal source (e.g. power device in board), high speed digital bus (e.g. memory bus), coil device (e.g. inductors) and wireless antenna (e.g. Bluetooth, WiFi, RF). It is recommended to place the chip close to the remote diode.

### $C_{IN}$, Pull-up resistor

It is better to place $C_{IN}$ as close as possible to VCC and GND pins of the chip. The recommended $C_{IN}$ value is 0.1 uF with low ESR ceramic cap although using multi caps, such as 1.0 uF plus 0.1 uF or 0.01 uF, is ok, which can suppress digital noise with different frequency range.

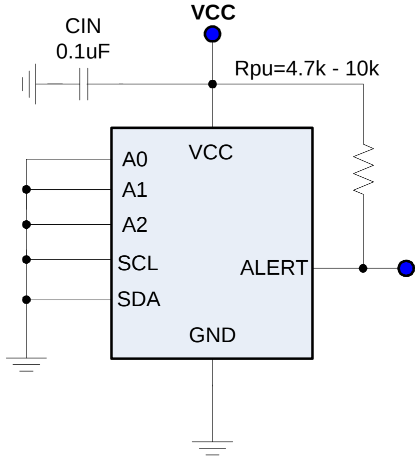
User has to put a pull-up resistor with 4.7 k to 10 k for SDA and SCL pins respectively. It is ok to use smaller resistors such as 2 k to 3 k in real application, if multi slave devices are used in the same bus.

### Standalone Thermostat

PJ85775 can also be used as standalone thermostat shown as below. It does not need external MCU to setup High/Low limitation temperature via SMBus/$I^2C$ communication. The trigger temperature and hysteresis temperature can be setup in factory before shipping to customer. For example,

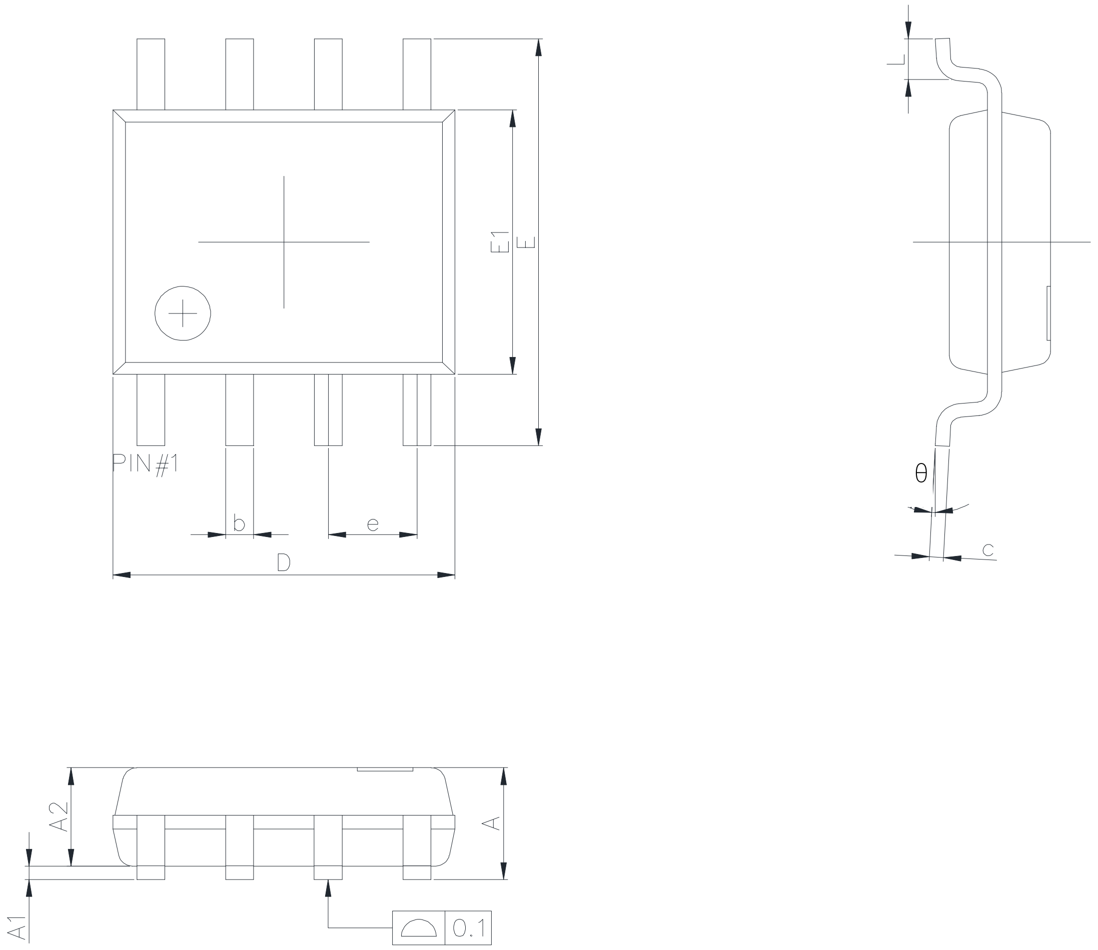
Trigger temperate is 55 °C, and Hysteresis temperature is 5 °C.

Which means when the chip temperature equals or exceeds 55 °C, the ALERT pin will be set low. And once the temperature of the chip drops below 50 °C (55 - 5), the ALERT pin will be released back to high (pulled by Rpu to VCC).



## PACKAGE OUTLINE DIMENSION (SOP-8)

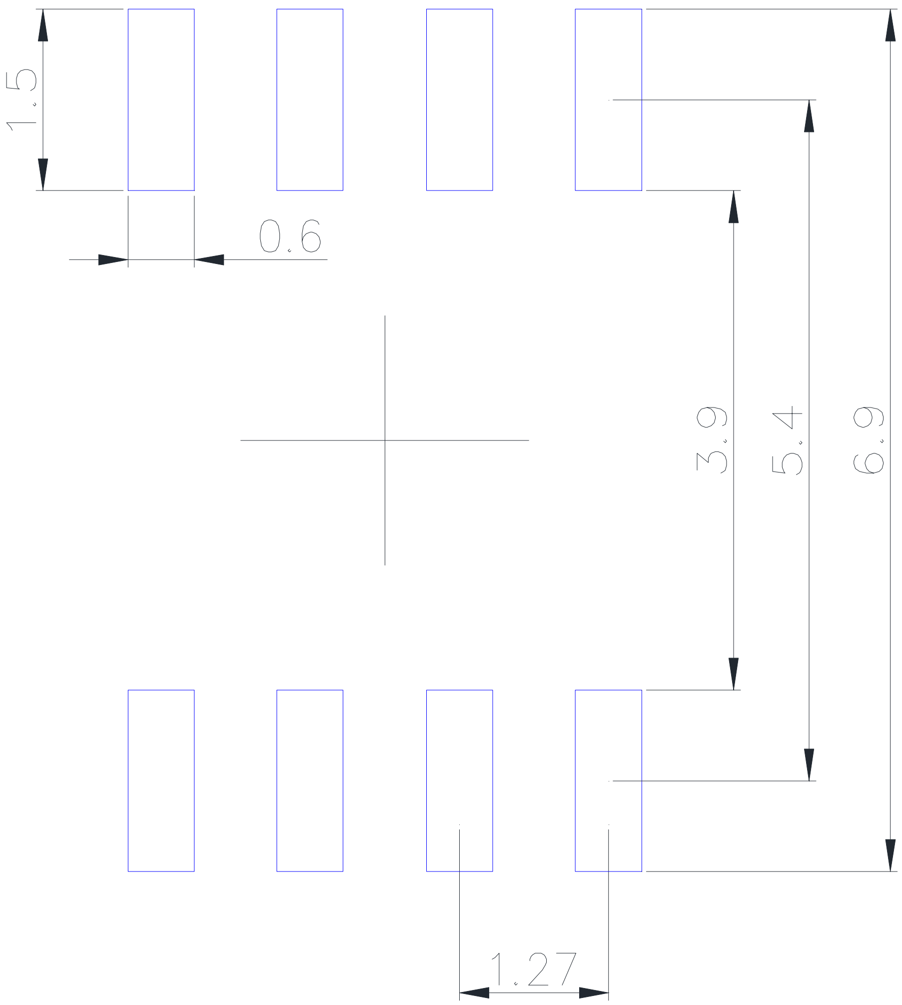
**SOP-8 Unit (mm)**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.250 | 1.650 | 0.049 | 0.065 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| c | 0.17 | 0.25 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.201 |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.700 | 4.100 | 0.146 | 0.161 |
| e | 1.270（BSC） | | 0.050（BSC） | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## Recommend Land Pattern Layout (SOP-8)

**SOP-8 Unit (mm)**

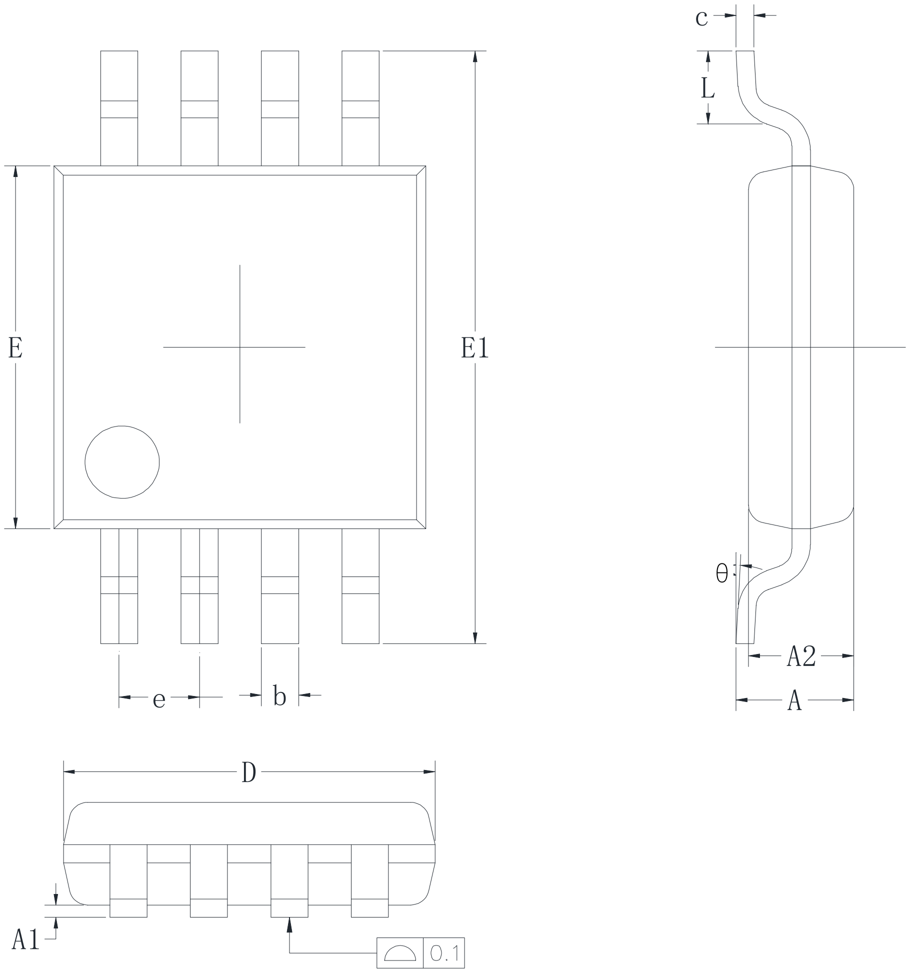



**Note:**

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. Change without notice

## PACKAGE OUTLINE DIMENSION (MSOP-8)

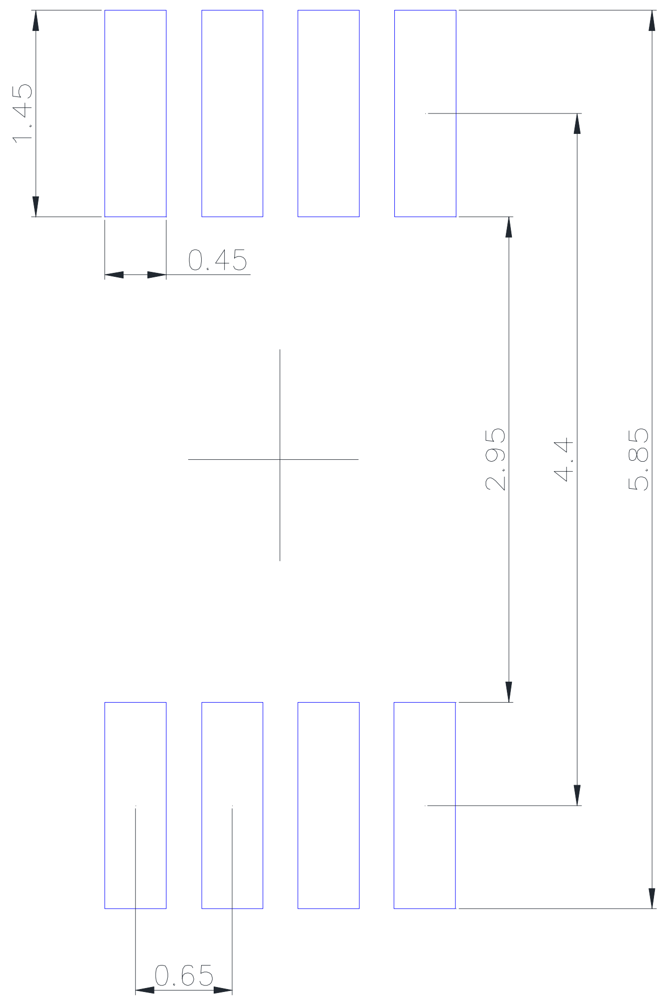
**MSOP-8 Unit (mm)**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.250 | 0.004 | 0.010 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.700 | 5.100 | 0.185 | 0.201 |
| e | 0.650（BSC） | | 0.026（BSC） | |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 8° | 0° | 8° |

## Recommend Land Pattern Layout (MSOP-8)

**MSOP-8 Unit (mm)**




**Note:**

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. Change without notice

# Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from Panjit International Inc..
- Panjit International Inc. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- Panjit International Inc. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- Panjit International Inc. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. Panjit International Inc. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments requiring high level of reliability or relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, transportation equipment, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panjit International Inc. for any damages resulting from such improper use or sale.
- Since Panjit uses lot number as the tracking base, please provide the lot number for tracking when complaining