PJ11027/F

18V, 2A, 600KHz High Efficiency Synchronous, Buck Converter In a SOT23-6 Package

GENERAL DESCRIPTION

PJ11027 is a simple and efficient integrated synchronous buck converter. It features a wide input voltage range of 4.5V to 18V, making it well-suited for various common input voltage rails such as 12V and 15V. It supports a continuous output current of up to 2A, with an output voltage range from 0.768V to 7V.

PJ11027 works in pulse frequency modulation (PFM) mode to maintain high efficiency under light loads; PJ11027F operates in forced pulse-width modulation (FPWM) mode to achieve a fixed switching frequency and low output ripple under full load current.

PJ11027 integrated comprehensive protection features, including input under-voltage protection (UVLO), per-cycle valley current limit protection (OCL), output under-voltage protection (UVP), output overvoltage protection (OVP), and over-temperature protection (OTP), to ensure its safe and reliable operation under various working conditions.

PJ11027 assemble in a compact SOT23-6 package and operates within a temperature range of -40°C to 125°C.

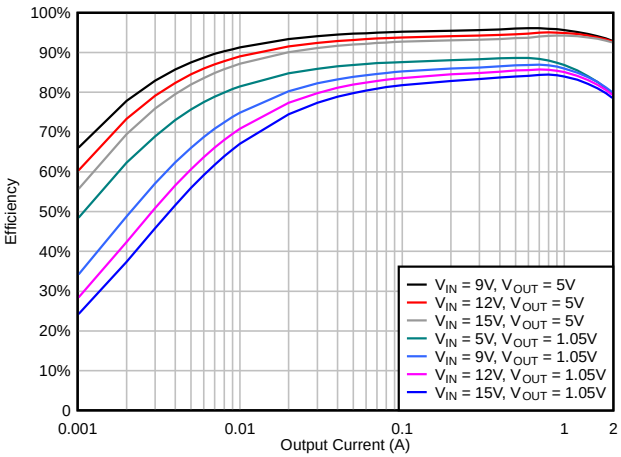
FEATURES

- Wide Operating Input Range: 4.5V to 18V
- Output Voltage Range: 0.768V to 7V
- Continuous Output Current: 2A
- Constant Switching Frequency: 600kHz
- 135mΩ / 70mΩ Low $R_{DS(ON)}$ Power MOSFETs
- Low quiescent current (I_Q)：190uA (Typ.)
- Low shutdown current (I_{SD})：2.5uA
- Fast load transient response by COT
- Optional Operation Modes Condition :
  - PJ11027 : Pulse Frequency Modulation (PFM)
  - PJ11027F : Forced Pulse Width Modulation (FPWM)
- High Reference Voltage Accuracy : 0.768V ±1.5%
- Complete Protections Integrated for Reliability:
  - Internal 1ms Soft-Start Avoiding Inrush Current
  - Cycle-by-Cycle Over Current Limit (OCL) : Peak Current Limit and Valley Current Limit
  - Unlatched VIN UVLO, OVP, UVP, OVP and OTP Protection
- Small Solution Size:
  - SOT23-6 Package

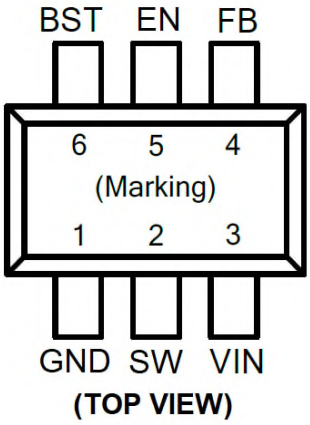
APPLICATIONS

- Digital Set-Top Box and Surveillance
- TV / Monitor
- EPOS
- Home Networking Device and Wireless Router
- Smart Speaker

TYPICAL EFFICIENCY CURVE



PIN CONFIGURATION



ORDERING INFORMATION

ORDER NUMBER	MODE	Marking ID	Package	Description
PJ11027S6_R1	PFM	A6 DNN	SOT23-6	Halogen Free in T&R, 3000 pcs/Reel
PJ11027FS6_R1	FPWM	A1 DNN	SOT23-6	Halogen Free in T&R, 3000 pcs/Reel

FUNCTIONAL PIN DESCRIPTION

TERMINAL		I/O(1)	DESCRIPTION
NUMBER	NAME		
1	GND	G	**Power Ground and Signal Ground.**
2	SW	P	**Switch Node.** Connect to power inductor with short and wide trace.
3	VIN	P	**Input Power Supply.** Add a 100nF ceramic decoupling capacitor as close to VIN and GND pins as possible.
4	FB	I	**Feedback Input**. Sense output voltage through the resistor divider for setting and controlling the output voltage.
5	EN	I	**Enable Control Pin**. Drive EN pin high to enable the device or low to disable the device.
6	BST	P	**Bootstrap Pin.** A capacitor rating 100nF must be connect from this pin to LX. It can be boost the gate drive to fully turn on the internal high side MOSFET.

(1) I – Input; O – Output; P – Power; G – Ground

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, SW	-0.3	19	V
	SW, Transient <10 ns	-3	21	V
	VIN – SW,	-0.3	19	V
	VIN – SW, Transient < 10 ns	-3	21	V
	BST	-0.3	25	V
	BST – SW	-0.3	6	V
	EN, FB	-0.3	6	V
T_J(2)	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	4.5		18	V
V_{OUT}	Output voltage range	0.768		7	V
F_{SW}	Buck switching frequency range		600		kHz
I_{OUT}	Output DC current range	0		2	A
T_J	Operating junction temperature	-40		125	°C

THERMAL INFORMATION

THERMAL RESISTANCE		SOT23-6	UNIT
Θ_{JA}(2)	Junction to ambient thermal resistance (JESD 51-7)	130.6	°C/W
Θ_{JB}	Junction to PCB thermal resistance	84.6	°C/W
Θ_{JC}	Junction to case thermal resistance	28.4	°C/W
$\Theta_{JA(EVM)}$(1)	Junction to ambient thermal resistance (Specific EVM)	69	°C/W

(1) $R_{\theta JA(EVM)}$ is based on the thermal resistance information measured during the actual operation of the corresponding evaluation Module. EVM information: 60mm x 45mm, FR-4, TG150, 1.6mm thickness, 2-layer 2-Oz Cu copper. Operating Condition: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A, T_A = 25°C. This thermal resistance information is for reference only. The actual thermal resistance depends on PCB board layout, and test environment conditions.

(2) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_{IN} = 12V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		18	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising	4.0	4.2	4.4	V
		V_{IN} falling	3.6	3.8	4.0	V
$I_{Q(VIN)}$	Quiescent current into the VIN pin, PJ11027	Non-switching, V_{EN} = 5 V, V_{FB} = V_{REF} x 105%, I_{OUT} = 0 A		190	220	μA
	Quiescent current into the VIN pin, PJ11027F	Non-switching, V_{EN} = 5 V, V_{FB} = V_{REF} x 105%, I_{OUT} = 0 A		193	220	μA
$I_{SD(VIN)}$	Shutdown current into the VIN pin	IC disabled, V_{IN} = 12V, V_{EN} = 0V		2.5	4.5	μA
EN						
$V_{EN(R)}$	EN input level to start switching	Rising threshold	1.15	1.21	1.27	V
$V_{EN(F)}$	EN input level to stop switching	Falling threshold	1.08	1.14	1.20	V
$I_{EN(P)}$	EN input current	V_{EN} = 1.0V	0.84	1.11	1.38	uA
$I_{EN(H)}$	EN hysteresis current		2.27	2.72	3.23	uA
FB						
V_{FB}	FB Voltage	T_J = 25 ℃	0.756	0.768	0.780	V
		T_J = -40 ℃ to 125 ℃, V_{IN} = 12V	0.753	0.768	0.783	V
$I_{FB(LKG)}$	FB Input Leakage Current	T_J = 25 ℃	-100	0	100	nA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARUP						
T_{SS}	Internal Fixed Soft-start Time	10% V_{OUT} to 90% V_{OUT}	0.5	1	1.5	mS
T_{DLY}	EN Delay Time	EN High to 1st Switching Pulse		400		uS
SWITCHING FREQUENCY						
F_{SW}	Switching Frequency, CCM Mode	V_{IN} = 12V, V_{OUT} = 1.05V, CCM		600		kHz
POWER STAGE						
$R_{DSON(HS)}$	High-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 12V, $V_{BOOT-SW}$ = 5V		135		mΩ
$R_{DSON(LS)}$	Low-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 12V, $V_{BOOT-SW}$ = 5V		70		mΩ
T_{ON_MIN}(1)	Minimum On Pulse Width			50		nS
T_{OFF_MIN}	Minimum Off Pulse Width			200		nS
T_{DEAD}	Dead Time			10		nS
I_{ZC}	Zero-cross detection current			80		mA
D_{MAX}	Maximum Duty			75		%
OVER CURRENT PROTECTION						
$I_{LS(OC)}$	Low-side Valley Current Limit	V_{IN} = 12V	2.7	3.1	3.5	A
$I_{LS(NOC)}$	Low-side Negative Current Limit, PJ11027F	V_{IN} = 12V	0.85	1.15	1.45	A
OUTPUT OVP AND UVP						
V_{OVP_HYS}	OVP Hysteresis			6.5		%
V_{OVP_R}	OVP Rising			115		%
V_{UVP_F}	UVP Failing			65		%
V_{UVP_HYS}	UVP Hysteresis			6.5		%
$T_{HCP(WAIT)}$	Wait Time before Entering UV Hiccup			110		uS
$T_{HCP(OFF)}$	UVP Hiccup Time before Re-startup			12		mS
OVER TEMPERATURE PROTECTION						
T_{SD}	Thermal shutdown temperature			150		°C
	Thermal shutdown hysteresis			30		°C

(1) Guaranteed by design

Typical Operating Characteristics

Test Conditions: V_{IN} = 12V, T_A = 25°C (unless otherwise noted)

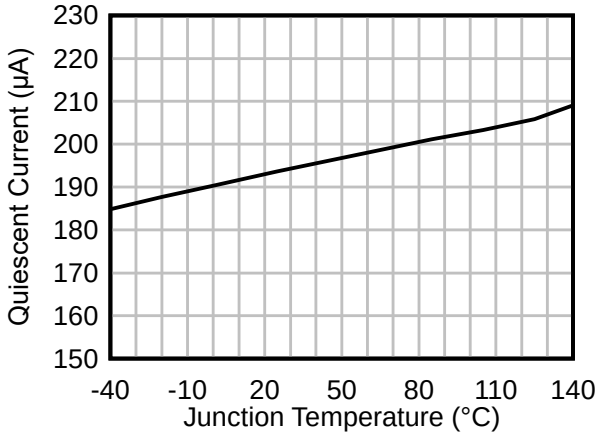


Figure-1. Quiescent Current (PJ11027) VS. Temp.

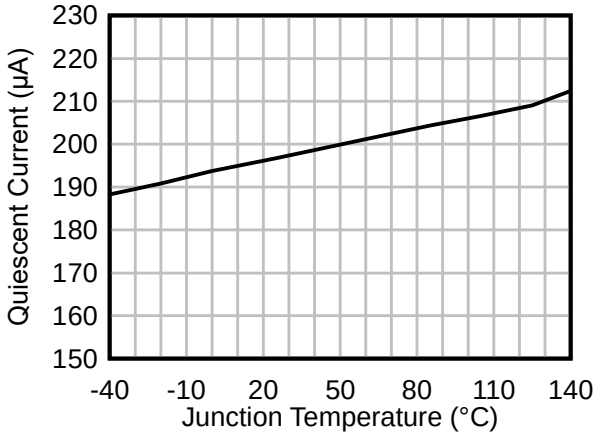


Figure-2. Quiescent Current (PJ11027F) VS. Temp.

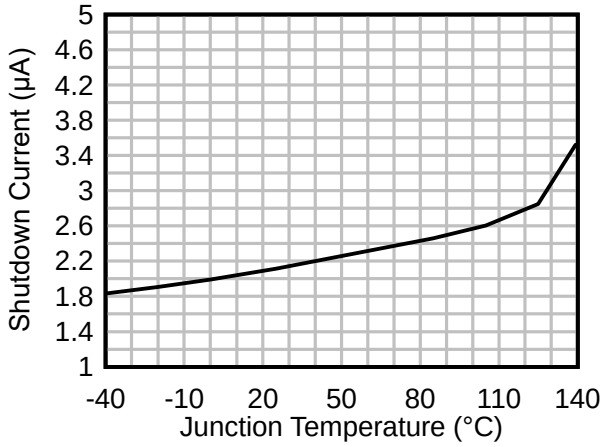


Figure-3. Shutdown Current VS. Temp.

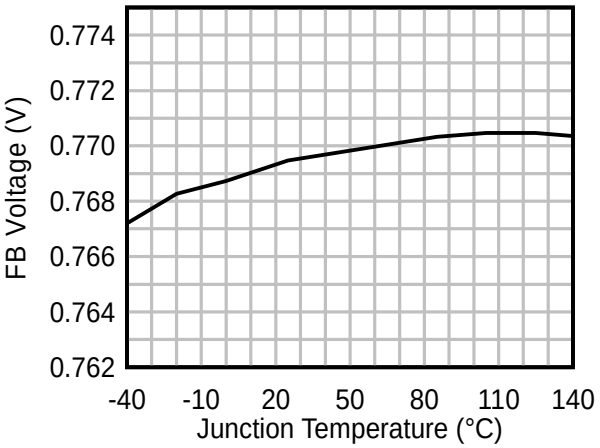


Figure-4. Reference Voltage VS. Temp.

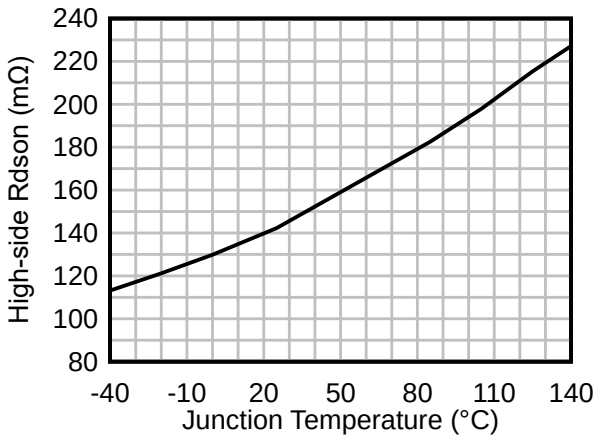


Figure-5. High-Side $R_{DS(ON)}$ VS. Temp.

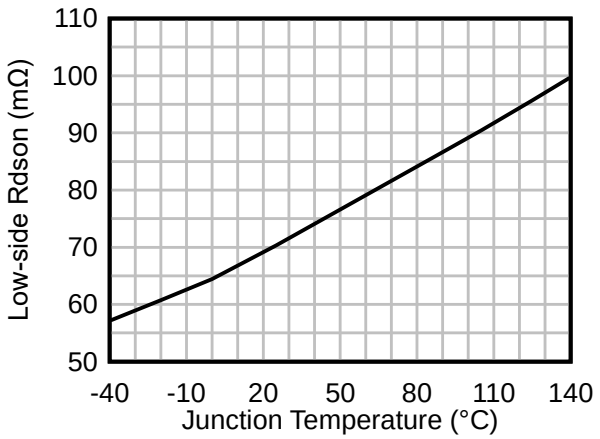


Figure-6. Low-Side $R_{DS(ON)}$ VS. Temp.

Test Conditions: V_{IN} = 12V, T_A = 25°C (unless otherwise noted)

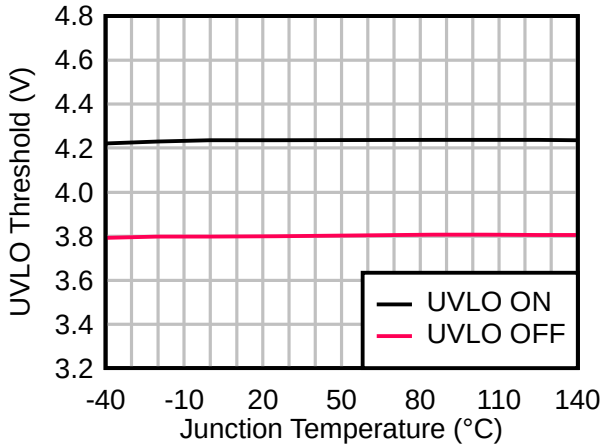


Figure-7. UVLO Threshold VS. Temp.

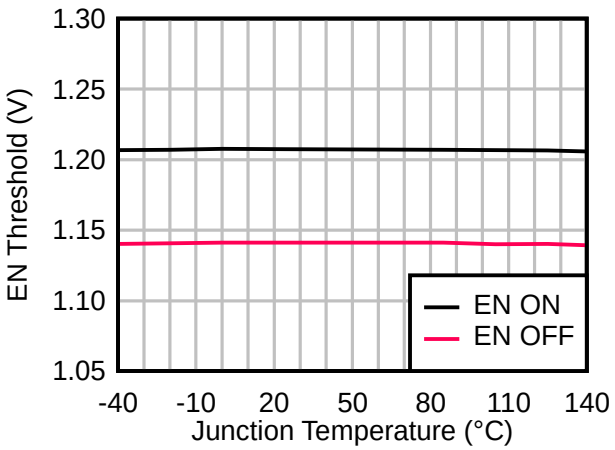


Figure-8. EN Pin Threshold VS. Temp.

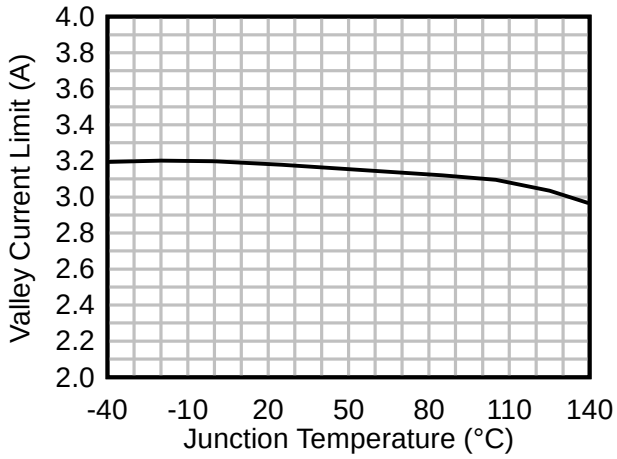


Figure-9. Valley Current Limit VS. Temp.

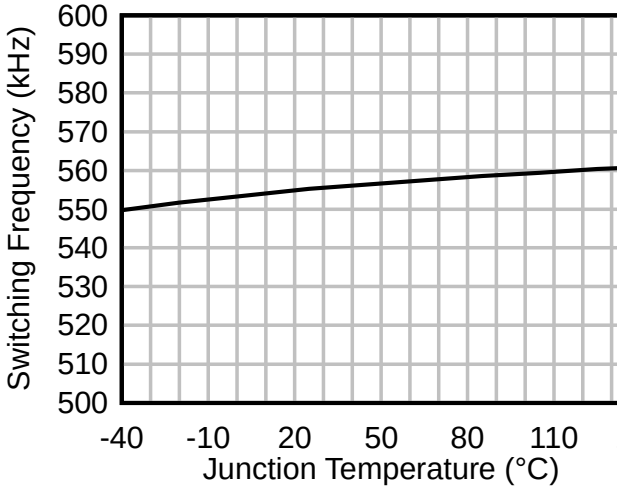


Figure-10. Switching Frequency VS. Temp.

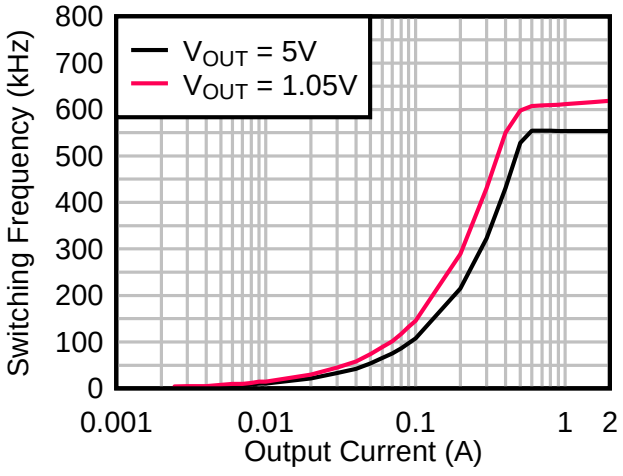


Figure-11. Switching Frequency (PJ11027) VS. I_{OUT}

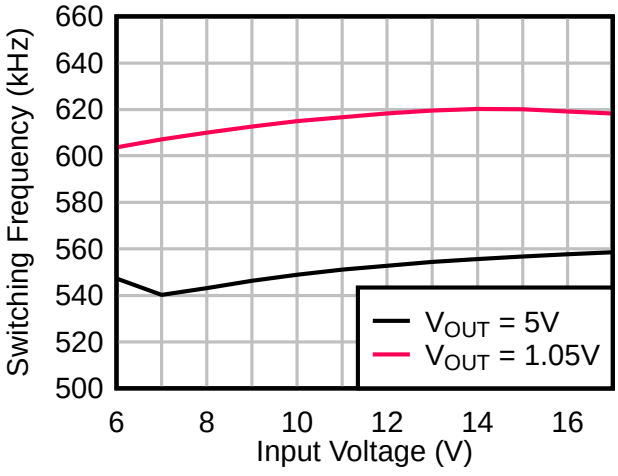
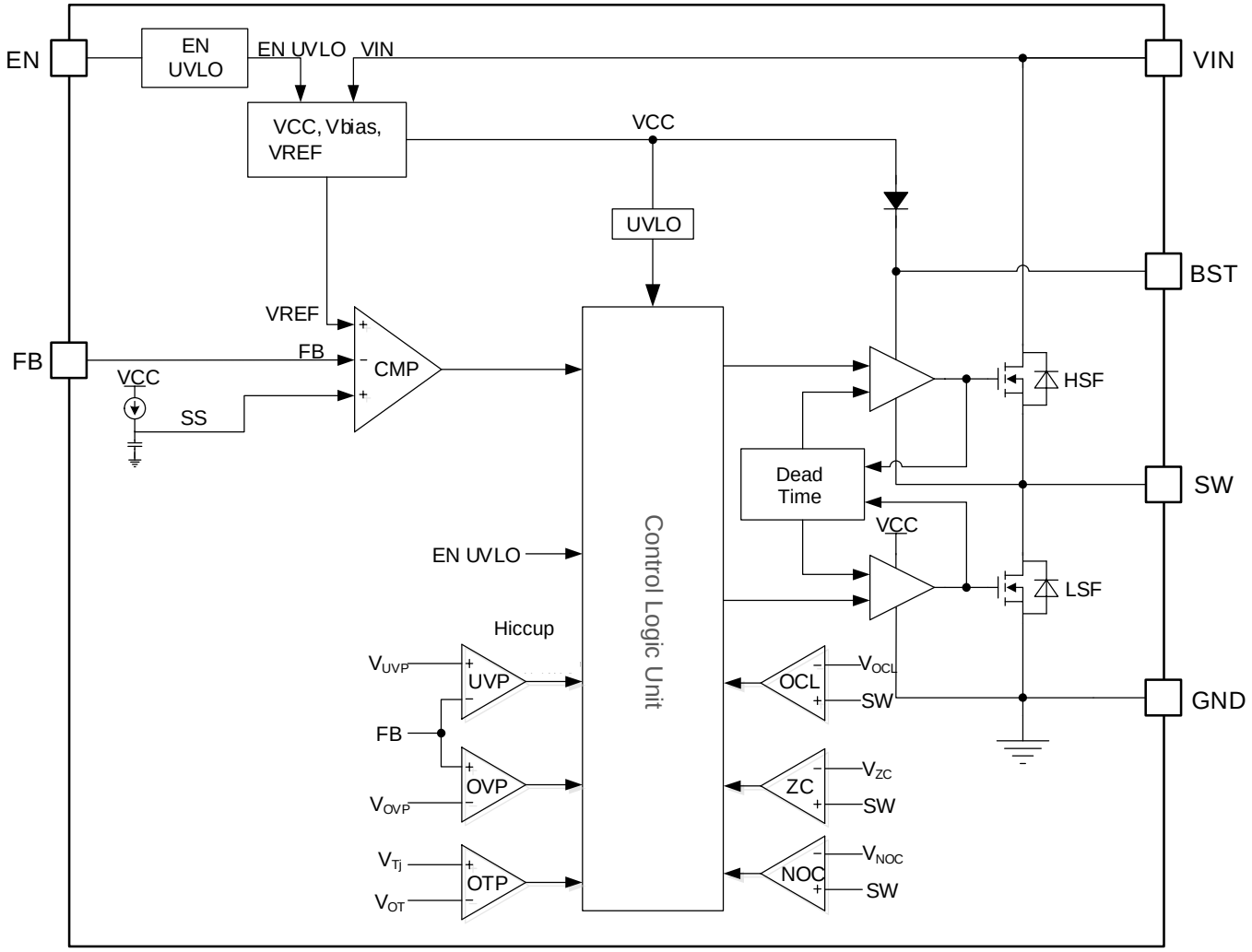


Figure-12. Switching Frequency (PJ11027F) VS. V_{IN}

FUNCTION BLOCK DIAGRAM



FEATURE DESCRIPTION

Overview

PJ11027 is a wide range of medium voltage input 4.5V-18V with 2A DC synchronous buck converter, especially for input voltage rails of 12V. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization, this helps designer save capacitance and reduces the cost of overall size. The internal on-time timer of PJ11027 is inversely proportional to the input voltage and directly proportional to the output voltage, allowing for a consistent operating frequency under various working conditions. Also integrates an additional output voltage error amplifier, capable of eliminating the DC output voltage offset caused by the half ripple of the COT control. This results got the higher output voltage accuracy and load regulation. During the light-load conditions, PJ11027 operates in Pulse Frequency Modulation (PFM) mode, maintaining high light-load output efficiency by reducing the switching frequency. On the other hand, PJ11027F operates in Forced Pulse Width Modulation (FPWM) mode, keeping a constant switching frequency to minimize output voltage ripple.

Device Operation Modes

Constant On-Time Control

PJ11027 employs Constant On-Time Control (COT) with a built-in voltage error integrator. COT control utilizes the output voltage valley ripple based on a comparator and on-time timer to achieve output voltage regulation.

At the beginning of each cycle, whenever the voltage on the feedback pin (FB) drops below the internal reference voltage, the internal high-side MOSFET (HS-FET) is turned on, it remains on for a fixed on-time duration before being turned off, and the on-time timer determines this on-time duration. The on-time timer is determined by both the output voltage and the input voltage to keep the switching frequency near constant over the full input voltage range. When the on-time timer has timed out, the HS-FET will remain off for at least 200ns (minimum turn-off time). After it, if the voltage on the feedback pin FB is lower than the internal reference voltage, the HSF will turn on again for a fixed on-time. By doing this, the converter achieves a quasi-constant frequency while maintaining a stable output voltage.

PJ11027 integrated a ripple injection circuit to simulate the output voltage ripple to achieve stable operation under low output ripple conditions with a low ESR ceramic output capacitor (MLCC). In addition, a ramp signal generation circuit is integrated to minimize switching jitter.

Pulse Frequency Modulation and Forced Pulse Width Modulation (FPWM)

PJ11027 automatically works in Pulse Frequency Modulation (PFM) mode under light load operation to maintain high efficiency at light loads. As the load current decreases, the valley of the inductor current ripple decreases until the inductor current valley drops to zero amps, which is the critical point between the continuous and discontinuous inductor current conduction modes - the inductor current critical conduction mode. Continuing to reduce the load current, PJ11027 will turn off the low-side MOSFET (LS-FET) when it detects that the inductor current has passed zero, thus keeping the inductor current at zero. In this case, the output capacitor is only discharged by the load current and the output voltage drops slower, thus the switching frequency will be reduced. As the switching frequency is reduced, the switching loss at light- load will also be reduced, which improves the light- load efficiency of the system.

PJ11027F works in forced pulse width modulation mode (FPWM) under light-load conditions to keep the switching frequency constant and maintain low output voltage ripple. When the HS-FET is off, the LS-FET is forced open after a dead time of 10ns until it closes before the HS-FET opens on the next cycle. This mode of operation does not detect the inductor current crossing point and allows the inductor current to flow through the drain-source terminal of the LS-FET from the output capacitor to the switching node, known as reverse current. In this case, the switching frequency remains nearly constant over the entire load current range, achieving low light-load output voltage ripple.

Precise Enable Control and UVLO

PJ11027 provides a chip external enable control pin (EN) to enable or disable chip operation. The chip is enabled for normal operation when the EN pin voltage exceeds the EN rising threshold voltage ($V_{EN(R)}$) and the V_{IN} voltage exceeds the V_{IN} under-voltage lockout threshold ($V_{UVLO(R)}$). If the EN pin voltage is pulled down below the threshold voltage ($V_{EN(F)}$), the chip stops switching and enters the shutdown mode, even if the VIN voltage is higher than the VIN under-voltage lockout threshold ($V_{UVLO(R)}$), the chip is disabled and the switching action stops. In shutdown mode, the chip's input current is reduced to the lowest shutdown current (2.5μA typical).

The EN pin has an internal pull-up current that allows the user to leave the EN pin open to enable the chip. Alternatively, depending on the application, the EN pin can be connected to an external logic controller to enable control of the chip. A 5V Zener diode (typical breakdown voltage 6.9V) is integrated into the EN pin to protect the internal circuits from over-voltage risk.

When externalizing the EN pin to voltages higher than 6V, such as VIN, a pull-up resistor (not less than 100kΩ) is added in series to limit the input current to the EN pin and prevent damage to the Zener diode, as shown in Figure below.

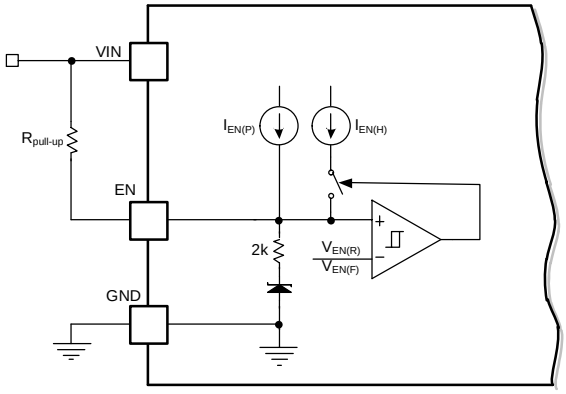


Figure-13. Pull-up Resistor to V_{IN}

The V_{IN} under-voltage lockout (UVLO) function prohibits the chip from operating when the input supply voltage is too low. The UVLO comparator monitors of the internal regulator, VCC. When V_{IN} drops below $V_{UVLO(F)}$, the chip stops switching and disables enable. When VIN rises up $V_{UVLO(R)}$, if V_{EN} is also greater than $V_{EN(R)}$ at that time, the chip will be enabled to start soft-start to resume normal operation.

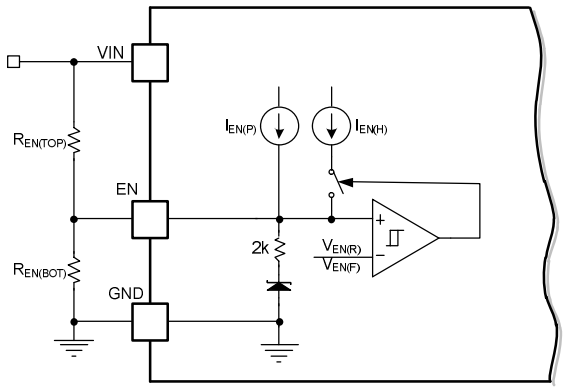


Figure-14. V_{IN} UVLO BLOCK

The V_{IN} UVLO rise and fall thresholds of the PJ11027 are fixed and the typical hysteresis voltage is 400 mV. If higher thresholds and hysteresis voltages are required in practical applications, the chip supports the customization of the V_{IN} UVLO rise and V_{IN} UVLO fall thresholds by connecting a voltage divider resistor to the EN pin to avoid repeated reboots of the chip due to the spike noise and ripples of the V_{IN} at the switch-on time. This prevents the chip from restarting repeatedly due to V_{IN} spike noise and ripple at the switch-on time, as shown in Figure-14.

The EN pin has an internal pull-up current ($I_{EN(P)}$) that enables the chip when the EN pin is externally suspended. The pull-up current can also be used to set the voltage threshold and hysteresis for the external V_{IN} UVLO function. The EN pin voltage, V_{EN}, is divided by V_{IN}, and as V_{EN} rises with V_{IN} and becomes greater than $V_{EN(R)}$, an additional pull-up hysteresis current ($I_{EN(H)}$) is turned on to change the ratio of the V_{EN} voltages, allowing for customized configurations of rising and falling thresholds. The $R_{EN(TOP)}$ and $R_{EN(BOT)}$ configurations for the specified V_{IN} UVLO thresholds can be calculated using Equation-1 and Equation-2 below, where $V_{IN(START)}$ and $V_{IN(STOP)}$ are the custom configured input startup and shutdown voltage values.

$$R_{EN(TOP)} = \frac{V_{IN(START)}\frac{V_{EN(F)}}{V_{EN(R)}} - V_{IN(STOP)}}{I_{EN(P)}\left(1 - \frac{V_{EN(F)}}{V_{EN(R)}}\right) + I_{EN(H)}}$$

Equation-1

$$R_{EN(BOT)} = \frac{R_{EN(TOP)}V_{EN(F)}}{V_{IN(STOP)} - V_{EN(F)} + R_{EN(TOP)}(I_{EN(P)} + I_{EN(H)})}$$

Equation-2

Soft Start and Pre-biased Soft Start

PJ11027 integrated an internal soft-start function to minimize the inrush current and ensure a smooth rise of the output voltage during the chip startup power-up process. When V_{IN} exceeds the UVLO threshold, the output voltage starts to rise after a delay of 440μs (typical) from the rising edge of EN. When the chip starts up, the internal soft-start circuitry generates a soft-start voltage (SS) that rises from zero. When SS is lower than the internal reference voltage (V_{REF}), SS overrides V_{REF}, so the voltage error integrator and control comparator use SS as the reference voltage, and the output voltage rises smoothly following SS. When SS rises to the V_{REF} voltage, V_{REF} regains control, the reference voltage stabilizes to V_{REF}, and

the output voltage then stabilizes to the set value V_{OUT}, and the soft-start is completed. The internal soft-start time, T_{SS} is fixed at 1ms, and is specified to be the time for the output voltage to rise from 10% to 90%.

If the output capacitor is already in a pre-biased voltage state when the chip starts up, PJ11027 activates the switch only after the internal reference voltage SS is greater than the feedback voltage V_{FB} and V_{OUT} starts to rise. This pre-bias soft-start scheme ensures that the chip's output voltage rises smoothly into a steady state.

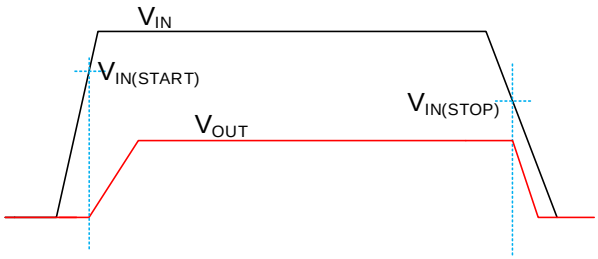


Figure-15. Start-up and Stop Voltage

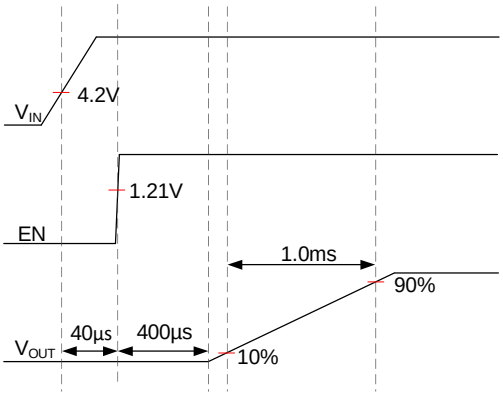


Figure-16. Soft-Start Timing Diagram

Output UVP with Hiccup mode

PJ11027 integrated an output under-voltage hiccup protection (UVP) that prevents the chip's outputs from being overloaded or shorted by constantly monitoring the feedback voltage V_{FB}. If V_{FB} lower than the output under-voltage protection threshold (V_{UVP}) (typically 65% of the internal feedback reference voltage), the output of the under-voltage comparator will be set high to shut down the internal high/low-side MOSFET, preventing the chip from continuing switching operation.

If the output under-voltage condition lasts longer than the fixed wait time ($T_{HCP(WAIT)}$), PJ11027 will enter output under-voltage protection (UVP) in hiccup mode. In hiccup mode, the chip will turn off the internal high-side and low-side MOSFET first for a fixed hiccup time ($T_{HICCUP(OFF)}$) and then attempt an automatic soft-start restart. After the soft-start is completed, if the fault condition is removed, the chip will resume normal operation; otherwise, it will continue to enter the hiccup protection and then automatic restart cycle until the fault condition is removed.

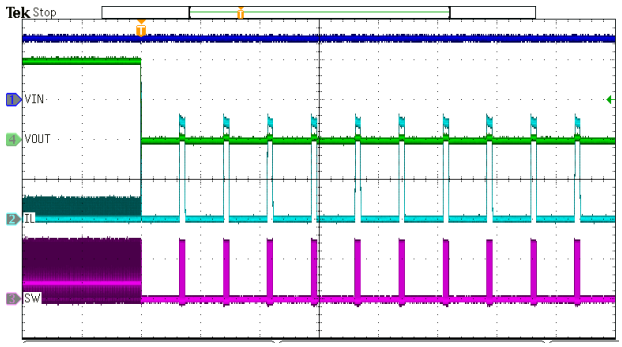


Figure-17. UVP Hiccup mode

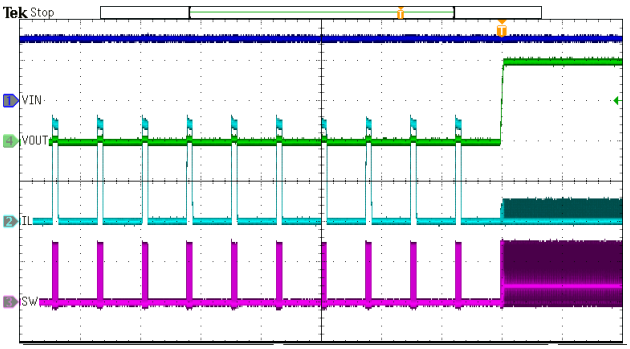


Figure-18. UVP Hiccup recovery

Peak and Valley Over-Current Limit

PJ11027 integrated valley current limit (OCL) protection. Whenever the internal low-side MOSFET on state, the chip detects the inductor current, and when the inductor current is greater than the current-limit threshold ($I_{LS(OC)}$), the current-limit comparator flips and PJ11027 enters the OCL mode.

At this time, the internal high-side MOSFET remains off until the inductor current drops below the current limit threshold ($I_{LS(OC)}$). If the load current of the chip exceeds the inductor current (inductor current is clamped by OCL), the output capacitor needs to supply additional current, thus the output capacitor discharges and the output voltage starts to drop. When the output voltage falls below the output under-voltage protection threshold (V_{UVP}), the chip stops operating and enters the UVP hiccup mode to avoid high temperature rise.

Negative Over-Current Limit (P11027F only)

PJ11027F works in FPWM mode under light-load conditions, which allows the low side MOSFET to pass reverse current. In FPWM mode, if the output is accidentally connected to an external power supply, the chip may operate in reverse boost mode, generating high reverse current to damage the chip PJ11027F integrated low-side MOSFET current detection circuitry, which immediately turns off the low-side MOSFET when it detects that the low-side MOSFET reverse current is greater than the threshold of inverse current limitation (NOC), and then turns on the high-side MOSFET to drain the output inductor of energy. Then the high-side MOSFET is turned on to drain the energy from the output inductor. This function protects the low-side MOSFET by limiting the reverse current above the NOC threshold, and the NOC current limit does not take effect during the minimum turn-off time.

Output Over-Voltage Protection

PJ11027 integrated an output over voltage protection (OVP) function to minimize output voltage overshoot and to protect downstream power equipment from damage caused by high voltage spikes that may occur during output fault conditions or sudden load reductions. The OVP circuitry detects overvoltage conditions by monitoring the feedback voltage (V_{FB}). When VFB exceeds the OVP threshold (V_{OVP}), the OVP comparator output goes high and both the built-in high-side and low-side MOSFETs shut down to prevent V_{OUT} from rising further. Once V_{OUT} falls below V_{OVP}, the chip starts working again. The output overvoltage protection function is non-latching.

Over Temperature Protection

PJ11027 is owned with an over temperature protection (OTP) function to prevent the chip from overheating due to excessive power dissipation. The internal circuitry of the chip detects the junction temperature of the chip, and when the junction temperature exceeds the over-temperature protection threshold ($T_{J(SD)}$), the OTP comparator flips and the chip stops the switching action, thus the junction temperature decreases. Once the junction temperature drops below the over-temperature protection hysteresis threshold ($T_{J(HYS)}$), the chip will resume normal operation and start soft start again.

APPLICATION INFORMATION

Overview

The output of the synchronous buck converter is mainly composed of inductors and capacitors, and the energy is stored and transferred to the load through the switching of the internally integrated power MOSFET, and a second-order low-pass filter is formed to smooth out the switching node voltage to obtain a stable output DC voltage. This section mainly describes the detailed design process based on the design example.

Output Voltage Setting

As shown in Figure-19., PJ11027 can be set to different output voltages by using an external divider resistor connected to the FB pin. The formula for the output voltage versus the external divider resistor is as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB(T)}}{R_{FB(B)}}\right) \qquad \textbf{Equation-3}$$

Where V_{REF} = 0.768V

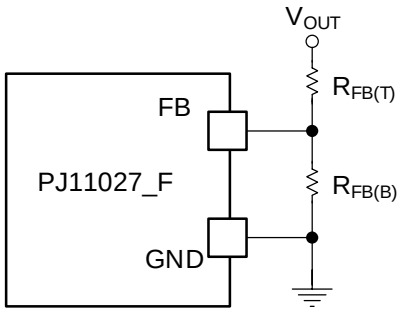


Figure-19. Output voltage setting

It is recommended to start the design with the voltage divider resistor $R_{FB(B)}$. Larger $R_{FB(B)}$ will cause the FB pin to be more susceptible to external noise interference, while too small RFB(B) will increase the power loss of the divider resistor. Considering both, it is recommended to choose $R_{FB(B)}$ = 10kΩ~50kΩ, and the voltage divider resistor $R_{FB(T)}$ can be calculated with Equation:

$$R_{FB(T)} = R_{FB(B)} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \qquad \textbf{Equation-4}$$

Where V_{REF} = 0.768V

For example, an output voltage of 5V, take $R_{FB(B)}$ to be 10kΩ and calculate $R_{FB(T)}$ to be 55.1kΩ, and select a nominal chip resistor of 54.9kΩ accordingly. For applications requiring high output voltage accuracy, 1% or higher precision voltage divider resistors are recommended.

PJ11027 is designed to work in the range of 4.5V to 18V. The buck converter requires an input voltage higher than the output voltage and with a recommended maximum operating duty cycle of 75%, the recommended minimum input voltage is V_{OUT}/0.75. The chip does not allow the output voltage to be higher than the input voltage, which is discharged through the high-side power body diode to the input supply. The resulting reverse current may cause unpredictable behavior. If such an application condition occurs, a diode by series, for example, can be added to block this reverse current.

Input Startup and Shutdown Voltage Setting

As shown in Figure-15. V_{IN} UVLO Threshold Setting and Figure-16. Input Startup Voltage and Shutdown Voltage Schematic, set the input startup voltage, $V_{IN(START)}$, and the input shutdown voltage, $V_{IN(STOP)}$, respectively, by configuring the EN divider resistor.

For example, 12V input voltage and 5V output voltage, the input startup voltage $V_{IN(START)}$ = 8V and the input shutdown voltage $V_{IN(STOP)}$ = 7V can be configured by selecting EN resistor. $I_{EN(P)}$ = 1.11μA, $I_{EN(H)}$ = 2.72μA into Equation-1 and Equation-2 to get $R_{EN(TOP)}$ = 215kΩ, $R_{EN(BOT)}$ = 36.5kΩ. For applications where the EN pin is directly controlled by a digital signal GPIO port, a GPIO port can be directly connected to the EN pin. If the chip does not start up when the GPIO port is in a high resistance state, it is recommended to add a pull-down resistor of less than 500kΩ to the EN pin.

Output Inductor Selection

Inductor selection based on the size, cost, efficiency and transient response performance of the chip solution. Three key parameters are considered: Inductance (L), Inductor Saturation current (I_{SAT}) and inductor DC resistance (DCR). As a compromise between inductor size and power consumption, it is recommended that the inductor be selected so that the ripple of the inductor current (ΔI_L) is 20% to 50% of the rated current (I_{rated}) of the PJ11027 as shown in the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{rated} \times K_L}$$

Equation-5

where

V_{IN} is input voltage,

V_{OUT} is output voltage,

f_{SW} is switching frequency,

I_{rated} is the rated current of 2A

K_L is the current ripple factor: 20%-50%

PJ11027 adopts COT control architecture and is optimized for common output voltages. It is recommended to refer to Table-1 directly for inductor selection. After selecting the inductance value according to Table-1, the actual inductor current ripple ΔI_L and peak value ($I_{L(peak)}$) can be calculated by the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

Equation-6

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Equation-7

where

$I_{OUT(MAX)}$ is the maximum output current

Select an inductor with a saturation current value ISAT that is at least greater than the inductor peak current IL(peak), and leave enough margin (e.g. 10%) to ensure that the inductor will not saturate during normal steady-state operation of the chip.

Due to the chip in the power-on startup, output overcurrent or load jump conditions, the inductor current may temporarily rise to greater than the peak current value IL(peak) in steady-state operation, at this time, a more conservative choice is to select the saturation current value ISAT is greater than the chip current limit IL(max_peak) inductor, to ensure that the inductor will not be saturated under any circumstances, check following equation.

$$I_{L(max\_peak)} = I_{LS(OC)} + \Delta I_L$$

Equation-8

Where

ILS(OC) is the valley current value of the chip

IL(max_peak) is the peak inductor current of the chip with the current limited in case

Considering that the output voltage of this example is 5V, a 4.7μH inductor is directly selected according to Table-1. Then the actual inductor ripple and peak current are:

$$\Delta I_L = \frac{5 \times (12 - 5)}{12 \times 580k \times 4.7\mu} = 1.07A$$

$$I_{L(peak)} = 2 + \frac{1.07}{2} = 2.535A$$

If a 4.7μH inductor is selected, make sure that the saturation current and rated current of the selected inductor are at least 2.535A. In addition, the peak inductor current can be calculated to take into account the load overcurrent:

$$I_{L(max\_peak)} = 3.1 + 1.07 = 4.17A$$

The most choice is to ensure that the saturation current of the selected inductor is greater than 4.17A.

Output Capacitor Selection

The selection of the output capacitor is related to the ripple of the output voltage and the voltage response performance when the load jumps. PJ11027 adopts the optimized COT control architecture after considering the actual application of ceramic capacitors, which achieves the ultra-fast load transient response and maintains the stable operation of the chip at the same time. In order to achieve the most suitable transient response performance, the recommended output capacitors and inductors are shown in Table-1:

V_{RIPPLE} output voltage ripple consists of two parts. One is the resistive ripple $V_{RIPPLE(ESR)}$ generated by the inductor current on the equivalent series resistance ESR of the output capacitor; the other one is the capacitive ripple $V_{RIPPLE(C)}$ generated by the inductor ripple current charging and discharging the output capacitor. The calculation equation as follows:

$$V_{RIPPLE} = \sqrt{V_{RIPPLE(ESR)}^2 + V_{RIPPLE(C)}^2} \quad \textbf{Equation-9}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times ESR \quad \textbf{Equation-10}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{sw}} \quad \textbf{Equation-11}$$

The actual ripple can simply be estimated as:

$$V_{RIPPLE} > Max\left(V_{RIPPLE(ESR)}, V_{RIPPLE(C)}\right)$$
$$V_{RIPPLE} < V_{RIPPLE(ESR)} + V_{RIPPLE(C)} \quad \textbf{Equation-12}$$

Considering this design example, two 22μF/16V ceramic capacitors are selected as the output capacitors according to Table-1. With the output voltage V_{OUT} = 5V, the actual total effective capacitance value is 14μF (7μFx2) and the actual equivalent ESR is 0.8mΩ (1.6mΩ/2), the output ripple V_{RIPPLE} can be calculated as follows:

$$V_{RIPPLE(ESR)} = 1.07 \times \frac{1.6m}{2} = 0.856mV$$

$$V_{RIPPLE(C)} = \frac{1.07}{8 \times 14\mu \times 580k} = 16.5mV$$

$$V_{RIPPLE} = \sqrt{16.5^2 + 0.856^2} = 16.52mV$$

Input Capacitor Selection

Since the input current of the buck converter is a pulsed discontinuous current, it is recommended to use a ceramic capacitor at the input to provide a pulsed input current thus keeping the DC input voltage stable. The ripple on the input capacitance of a ceramic capacitor can be calculated by the following equation:

$$V_{IN(Ripple)} \approx D \times I_{OUT} \times \frac{1 - D}{C_{IN} \times f_{sw}} + I_{OUT} \times ESR$$

Equation-13

Where $D = \frac{V_{OUT}}{V_{IN}}$

In addition, since the input capacitance is a pulsed discontinuous current, the selected input capacitor must be able to withstand a large AC current:

$$I_{IN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D(1 - D)} \quad \textbf{Equation-14}$$

In order to optimize the EMI performance of the chip and to ensure reliable and stable, it is recommended to add a 0.1μF ceramic capacitor (0603/0402 package) in addition to the ceramic capacitor as input capacitance C_{IN}, and place it as close as possible to the VIN and GND pins of the chip. It should be noted that although ceramic capacitors have excellent high frequency performance and stable lifetime, in some hot-swap scenarios, the actual V_{IN} voltage may oscillate due to the low ESR of the ceramic capacitors, and in the worst case, it may oscillate up to 2 times the V_{IN} voltage, which can cause over-voltage breakdown of the chip. In this case, it is recommended to add an additional electrolytic capacitor with a larger ESR or a TVS diode in parallel with the input voltage to limit the input overvoltage.

Table-1 Recommended Component Selection Table

V_{OUT} (V)	$R_{FB(T)}$ (kΩ)	$R_{FB(B)}$ (kΩ)	L_{min} (μH)	L_{typ} (μH)	L_{max} (μH)	$C_{OUT(EFF)}$ (μF)
5.0	54.9	10	3.3	4.7	5.6	10 to 68
3.3	33.2	10	2.2	3.3	4.7	10 to 68
2.5	22.6	10	2.2	2.2	4.7	20 to 68
1.8	13.7	10	1.5	2.2	4.7	20 to 68
1.5	9.53	10	1.5	1.5	4.7	20 to 68
1.2	5.76	10	1.2	1.5	4.7	20 to 68
1.05	3.74	10	1.0	1.5	4.7	20 to 68
1	3.09	10	1.0	1.5	4.7	20 to 68

Feedforward Capacitor Selection

PJ11027 utilizes the COT control architecture to achieve ultra-fast load transient response performance. In some applications where the load transient response is more demanding, the transient response can be further improved by adding a R_{FF}, and a C_{FF}, to the output feedback divider resistor. Considering the influence of noise coupling, it is recommended to use R_{FF} = 2 kΩ~10 kΩ, and do not use C_{FF} higher than 100 pF. Note that the actual R_{FF} and C_{FF} are optional devices, and it is recommended to optimize the selection based on the results of the measured load transient response and the output tuning rate.

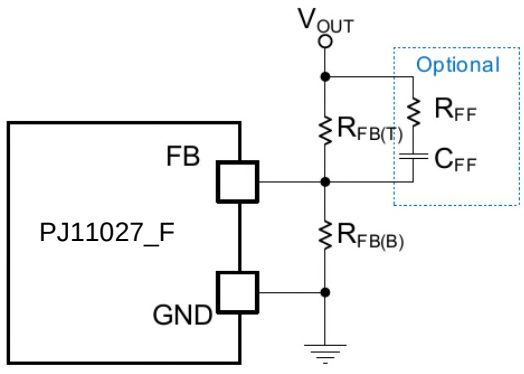


Figure-20. Feedforward Resistor and Capacitor

PCB Design Guidelines

The stability of the device operation greatly depends on the PCB layout.

1. Position the ceramic capacitors as close to the VIN and GND pins as possible.

2. Keep the alignment of the power circuit (CIN→L→COUT→GND) as short and wide as possible to minimizes circuit voltage drop and enhances conversion efficiency.

3. The voltage waveform of the SW node forms a high-frequency square wave. Appropriately reducing the copper spreading of the SW node can enhance EMI performance. Conversely, increasing the spreading can optimize heat dissipation. The user should make the appropriate decision considering these factors based on the actual situation.

4. Leave a considerable distance between the FB pin and noise sources like the SW node and BST node.

5. Place the sampling point of the output voltage VOUT close to the end of the output capacitor, and position the voltage divider sampling resistor near the FB pin.

6. Route and spread the copper of VIN and GND as wide as possible to help heat dissipation. In multilayer PCB design, it is recommended to have a complete GND layer for the GND pin and to add enough vias between the GND layer and the chip layer.

PCB design example is shown below:

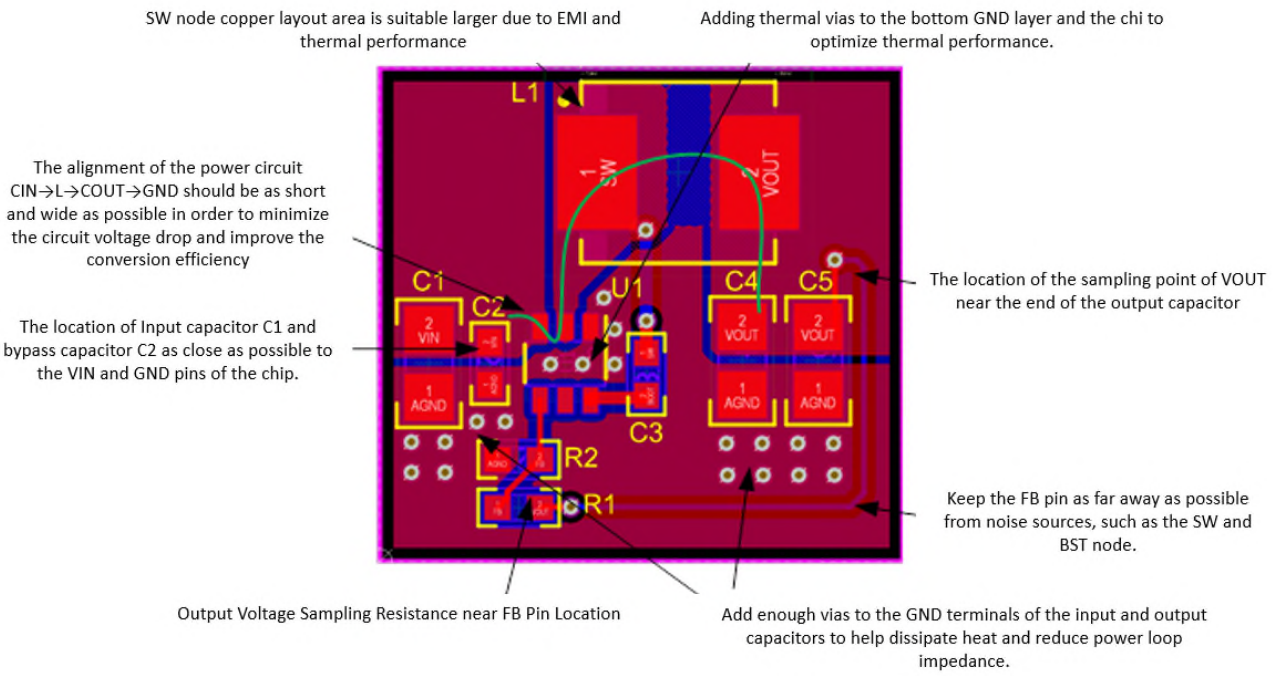


Figure-21. PCB Design Example

Typical Reference Design

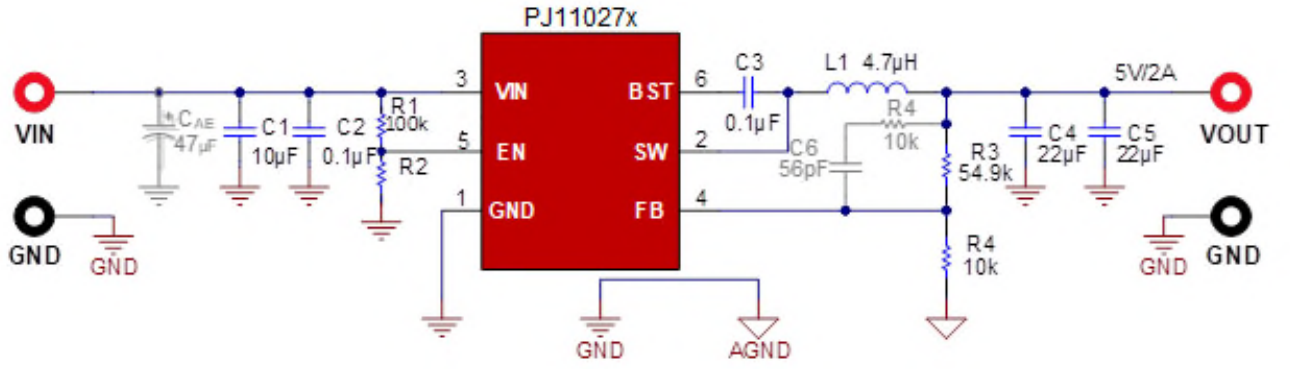


Figure-22. V_{IN}= 12V, V_{OUT}= 5V, I_{OUT}= 2A

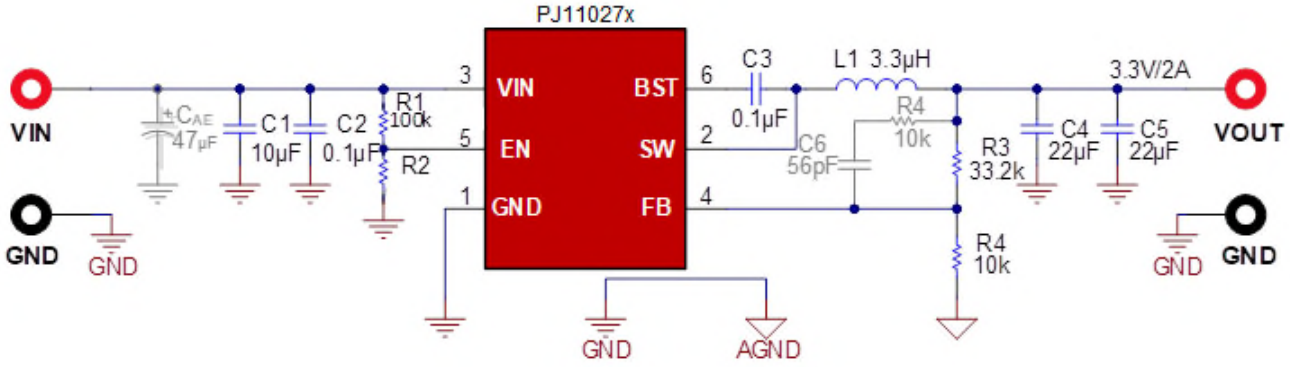


Figure-23. V_{IN}= 12V, V_{OUT}= 3.3V, I_{OUT}= 2A

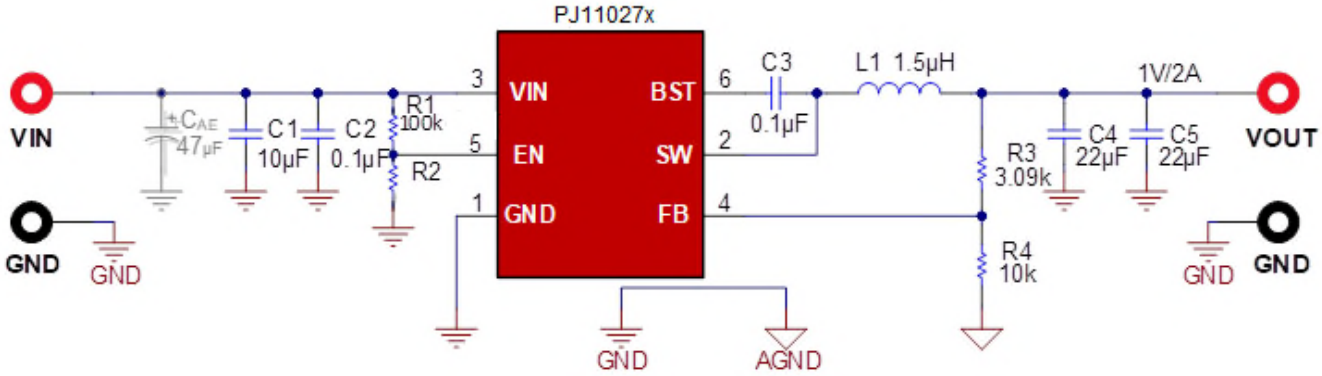


Figure-24. V_{IN}= 12V, V_{OUT}= 1.0V, I_{OUT}= 2A

Typical Operating Characteristics

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

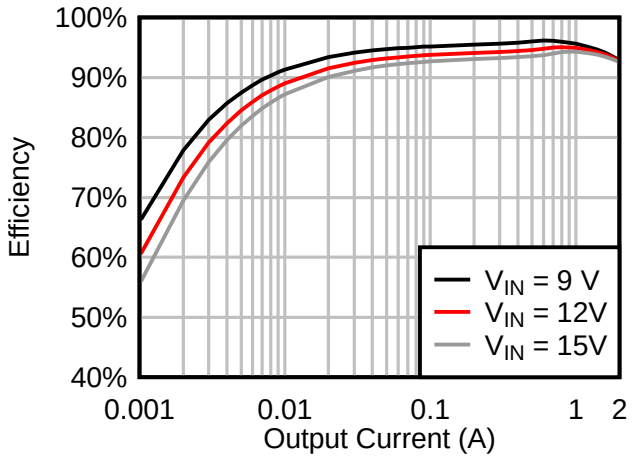


Figure-25. PJ11027 V_{OUT} = 5V Efficiency

L = 4.7µH, DCR = 33mΩ

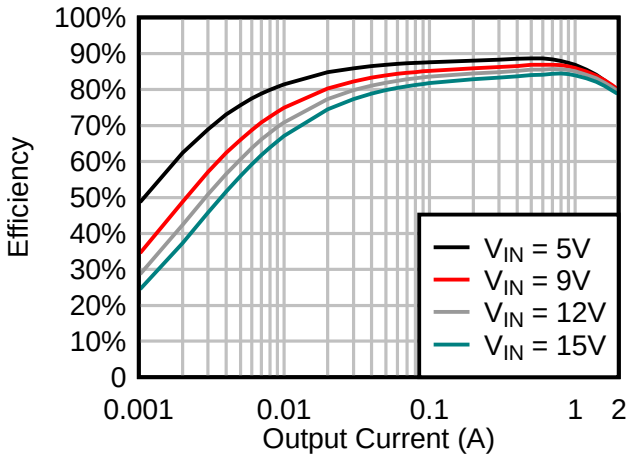


Figure-26. PJ11027 V_{OUT} = 1.05V Efficiency

L = 1.5µH, DCR = 12mΩ

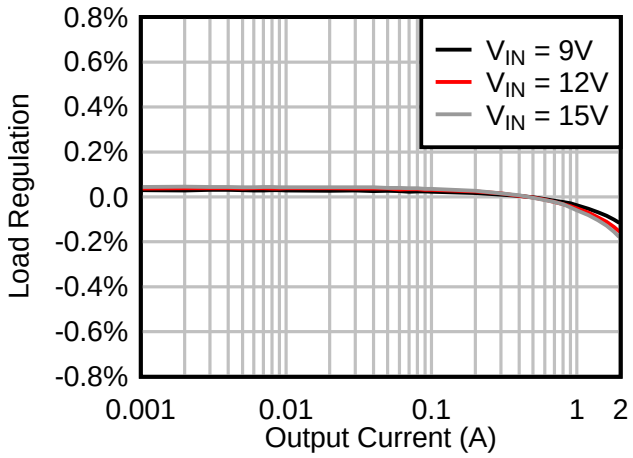


Figure-27. PJ11027 Load Regulation V_{OUT} = 5V

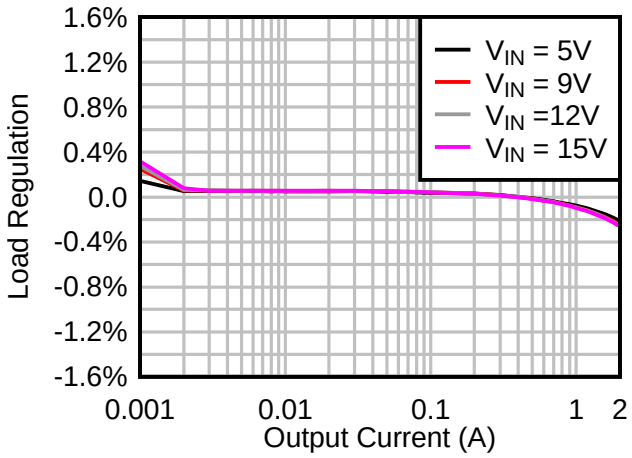


Figure-28. PJ11027 Load Regulation V_{OUT} = 1.05V

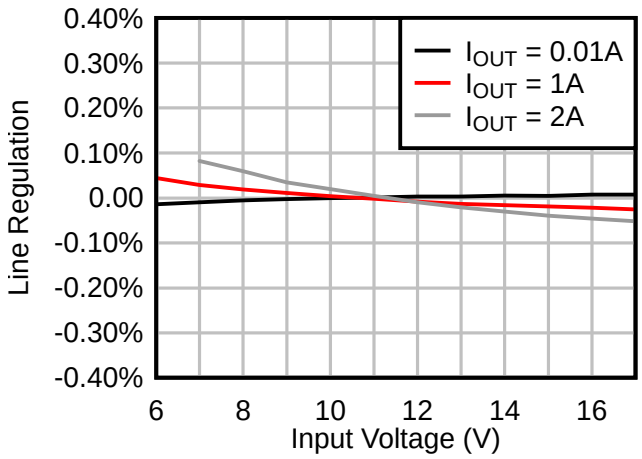


Figure-29. PJ11027 Line Regulation V_{OUT} = 5V

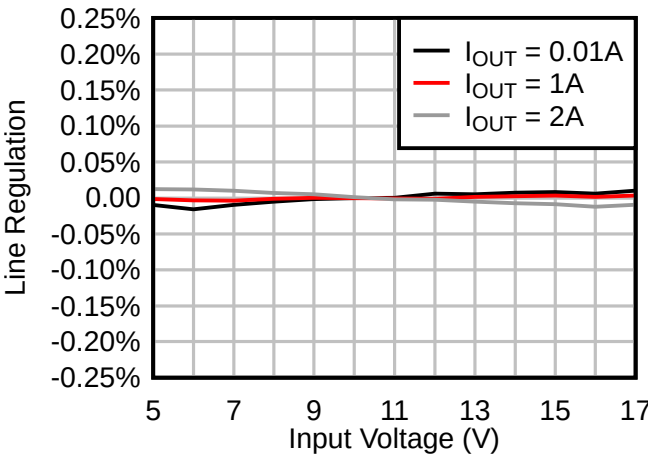


Figure-30. PJ11027 Line Regulation V_{OUT} = 1.05V

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

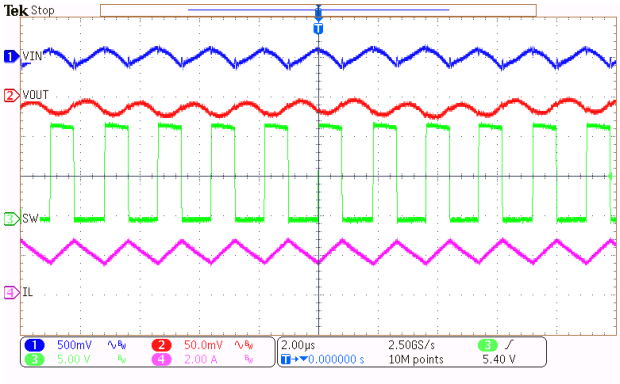


Figure-31. Input Ripple, I_{OUT} = 2A

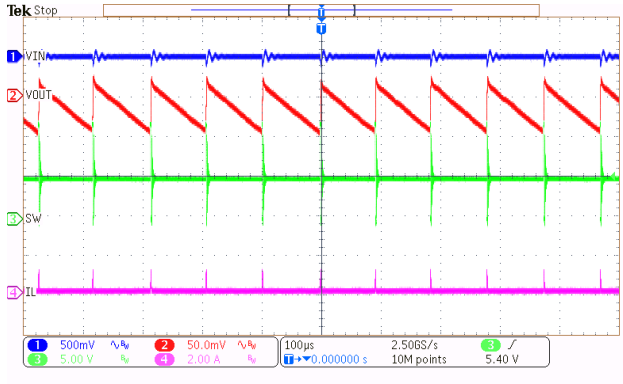


Figure-32. Output Ripple, I_{OUT} = 10mA

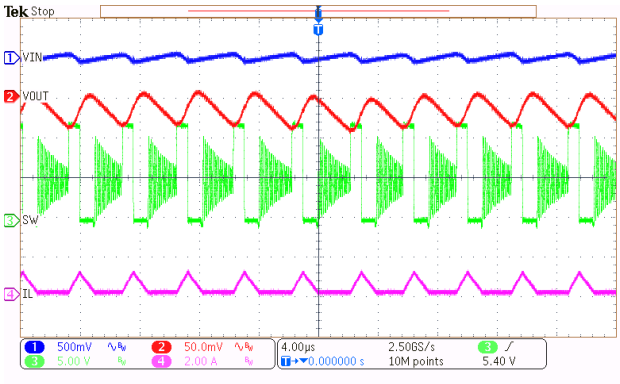


Figure-33. Output Ripple, I_{OUT} = 250mA

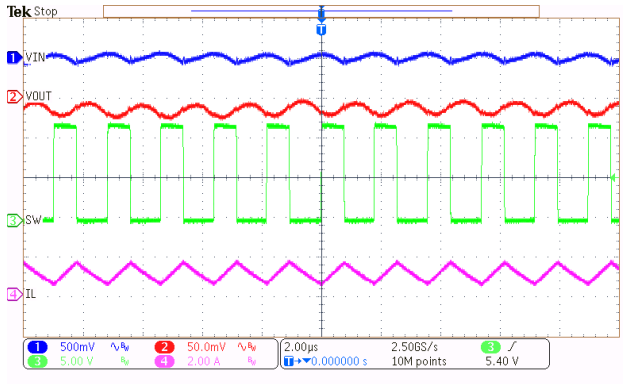


Figure-34. Output Ripple, I_{OUT} = 1A

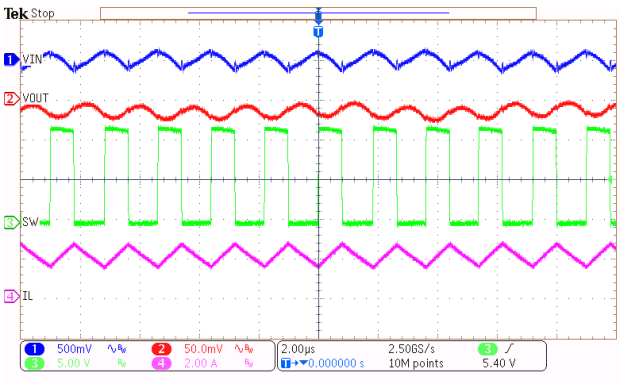


Figure-35. Output Ripple, IOUT = 2A

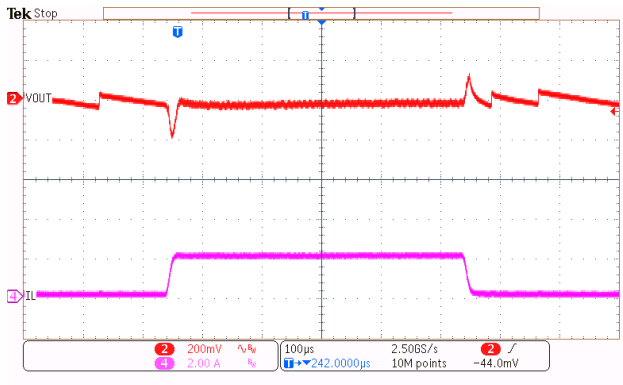


Figure-36. Load Transient, IOUT = 0A-2A, 250mA/µs

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

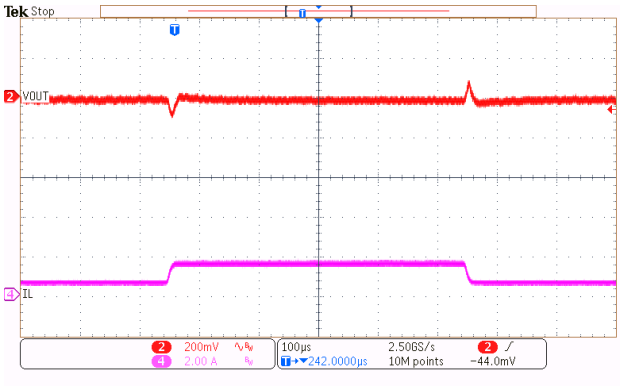


Figure-37. Load Transient Response, I_{OUT} = 0.5A-1.5A, 250mA/µs

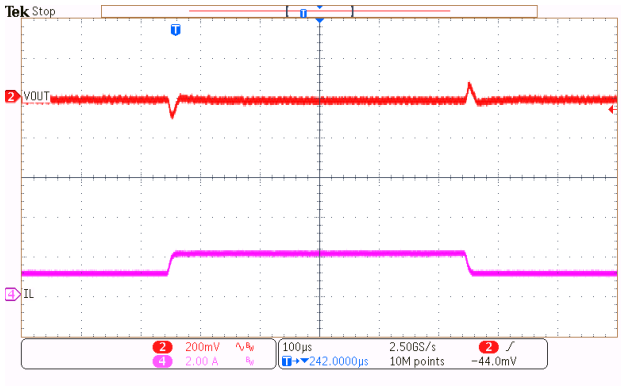


Figure-38. Load Transient Response, I_{OUT} = 1A-2A, 250mA/µs

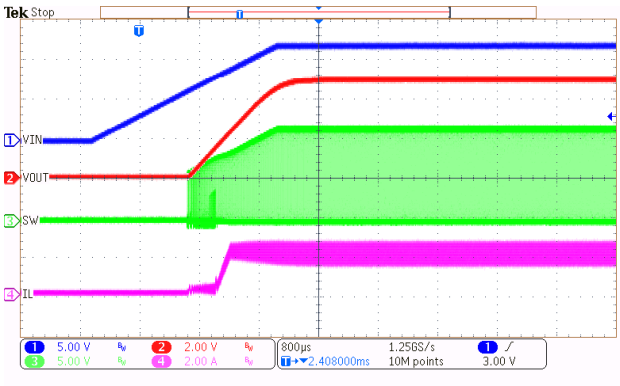


Figure-39. Start-Up, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A

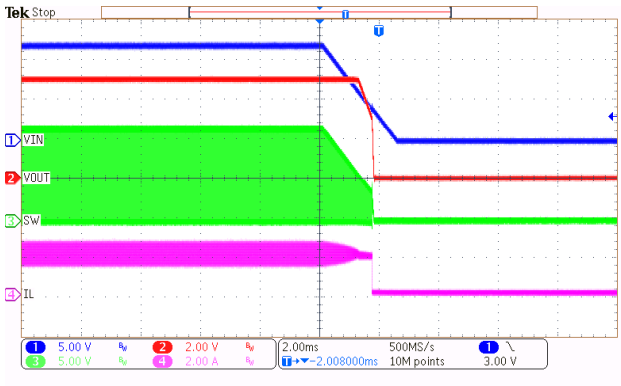


Figure-40. Shut-Down, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A

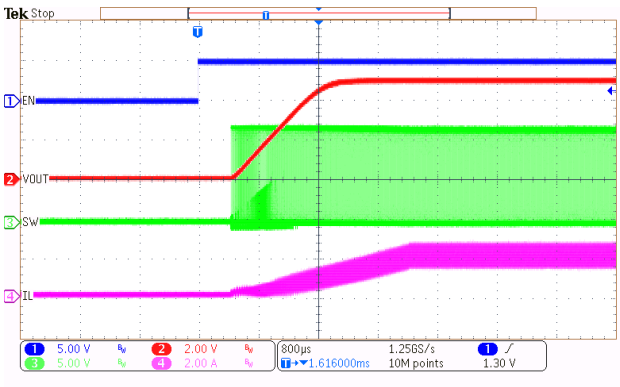


Figure-41. Start-Up, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A

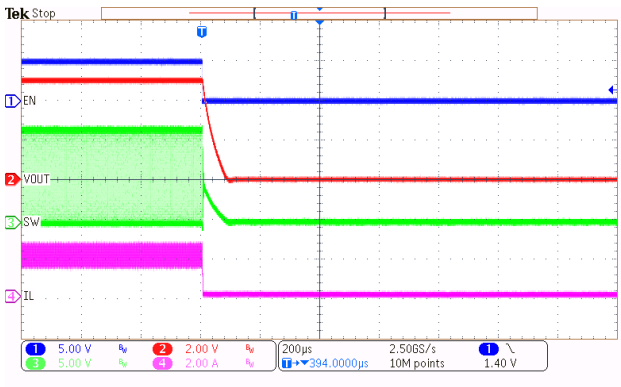
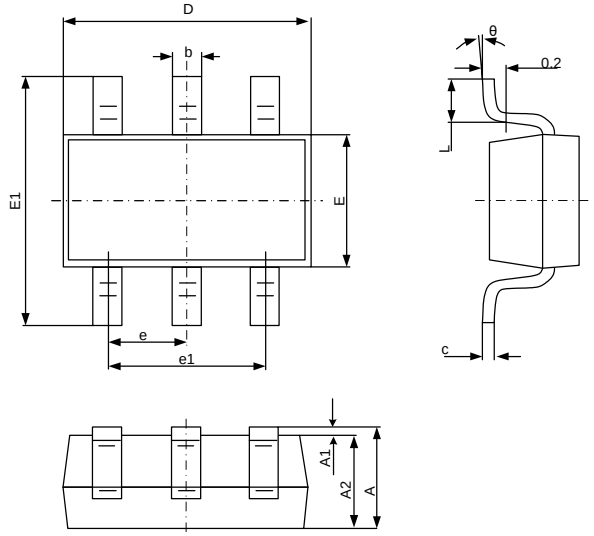


Figure-42. Shut-Down, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A

PACKAGE DIMENSION

SOT23-6



Symbol	Dimensions (Millimeters)		Dimensions (Inches)	
	Min.	Max.	Min.	Max.
A	-	1.350	-	0.053
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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