PJ10515/F

5.5V, 1.5A, 1.5MHz High Efficiency Synchronous, Buck Converter In a SOT23-5 Package

GENERAL DESCRIPTION

PJ10515/F is high efficiency, synchronous Buck converter with integrated MOSFETs. It operates with 1.5MHz switching frequency and the input supply voltage range of 2.5V to 5.5V, and supports up to 1.5A continuous output current. The duty cycle is up to 100% for the lowest dropout.

At light load, PJ10515 operates in PFM to maintain high efficiency, and PJ10515F operates in FPWM to maintain tight output voltage ripples.

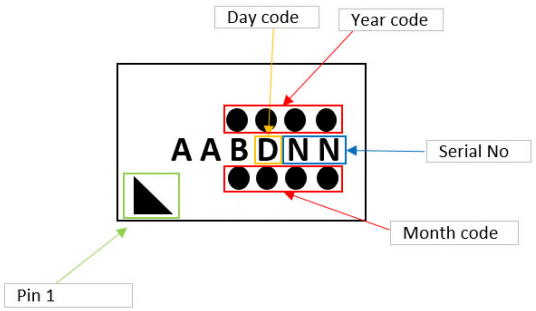
PJ10515/F integrates complete protection features including input under-voltage lock-out (UVLO), input over-voltage protection (OVP), cycle-by-cycle over current limit (OCL), output under-voltage protection with hiccup (UVP), output over-voltage protection (OVP) and over-temperature protection (OTP) to confirm its safe and stable operation at different conditions.

PJ10515/F is available in SOT23-5 package and the junction temperature is specified from -40°C to 125°C.

FEATURES

- 2.5V to 5.5V Input Voltage Range
- 1.5A Continuous Output Current
- 1.5MHz CCM Switching Frequency
- Support Maximum Duty Cycle : 100%
- Low Quiescent Current: 45μA
- Low Shutdown Current: 0.1μA
- Peak Current Mode (PCM) Control
- Optional Operation Modes Condition :
  - PJ10515 : Pulse Frequency Modulation (PFM)
  - PJ10515F : Forced Pulse Width Modulation (FPWM)
- High Reference Voltage Accuracy : 0.6V ±1.0%
- Complete Protections Integrated for Reliability:
  - Internal 0.5ms Soft-Start Avoiding Inrush Current
  - Cycle-by-Cycle Over Current Limit (OCL) : Peak Current Limit and Valley Current Limit
  - Unlatched VIN UVLO, VIN OVP, UVP, OVP and OTP Protection
- Small Solution Size:
  - Small MLCC Output Capacitors Supported
  - No External Compensation Needed
  - SOT23-5 Package

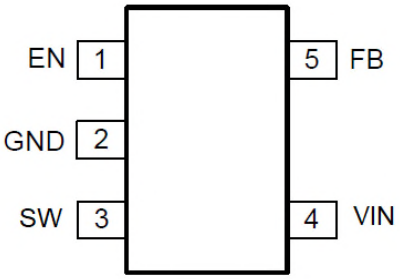
MARKING INFORMATION



APPLICATIONS

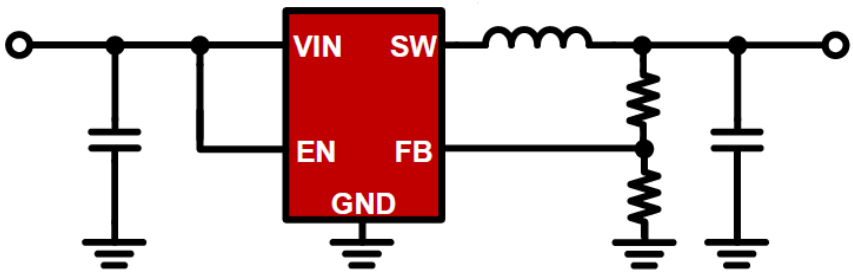
- Digital Set-Top Box and Surveillance
- TV / Monitor and EPOS
- Home Networking Device and Wireless Router
- Smart Speaker
- 5V/3.3V Distributed Power Systems

PIN CONFIGURATION



(TOP VIEW)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION

ORDER NUMBER	Operation Mode	Marking ID	Package	Description
PJ10515S5_R1	PFM	A1BDNN	SOT23-5	Halogen Free in T&R, 3000 pcs/Reel
PJ10515FS5_R1	FPWM	AEBDNN	SOT23-5	Halogen Free in T&R, 3000 pcs/Reel

FUNCTIONAL PIN DESCRIPTION

TERMINAL		I/O(1)	DESCRIPTION
NUMBER	NAME		
1	EN	I	**Enable Control Pin**. Drive EN pin high to enable the device or low to disable the device. Do not leave EN pin floating.
2	GND	G	**Power Ground and Signal Ground.**
3	SW	P	**Switch Node.** Connect to power inductor with short and wide trace.
4	VIN	P	**Input Power Supply.** Add a 100nF ceramic decoupling capacitor as close to VIN and GND pins as possible.
5	FB	I	**Feedback Input**. Sense output voltage through the resistor divider for setting and controlling the output voltage.

(1) I – Input; O – Output; P – Power; G – Ground

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, EN	-0.3	6	V
	SW, DC	-0.3	V_{IN}+0.3	V
	SW, Transient <10 ns	-3	9	V
	FB	-0.3	5.5	V
T_J(2)	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		V_{IN}	V
F_{SW}	Buck switching frequency range		1500		kHz
I_{OUT}	Output DC current range	0		1.5	A
T_J	Operating junction temperature	-40		125	°C

THERMAL INFORMATION

THERMAL RESISTANCE		SOT23-5	UNIT
Θ_{JA}(1)	Junction to ambient thermal resistance (Specific EVM)	65	°C/W

(1) $R_{\theta JA(EVM)}$ is based on the thermal resistance information measured during the actual operation of the corresponding evaluation Module. EVM information: 60mm x 45mm, FR-4, TG150, 1.6mm thickness, 2-layer 2-Oz Cu copper. Operating Condition: V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 1.5A, T_A = 25°C. This thermal resistance information is for reference only. The actual thermal resistance depends on PCB board layout, and test environment conditions.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 150°C, V_{IN} = 5V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		2.5		5.5	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.3	2.4	2.5	V
		V_{IN} falling	2.1	2.2	2.3	V
		V_{IN} Hysteresis		0.2		V
I_Q	Quiescent current into the VIN pin, PJ10515	Non-switching, V_{EN} = 5 V, V_{FB} = V_{REF}*105%, I_{OUT} = 0 A		45		μA
	Quiescent current into the VIN pin, PJ10515F	Non-switching, V_{EN} = 5 V, V_{FB} = V_{REF}*105%, I_{OUT} = 0 A		50		μA
I_{SD}	Shutdown current into the VIN pin	IC disabled, V_{IN} = 5V, V_{EN} = 0V		0.1		μA
EN						
$V_{EN\_H\_R}$	EN input level to start switching	Rising threshold		0.88	1.15	V
$V_{EN\_H\_F}$	EN input level to stop switching	Falling threshold	0.5	0.75		V
FB						
V_{FB}	FB Voltage	T_J = 25 ℃	0.594	0.6	0.606	V
		T_J = -40 ℃ to 125 ℃	0.591	0.6	0.609	V
$I_{FB(LKG)}$	FB Input Leakage Current	T_J = 25 ℃	-100	0	100	nA
STARUP						
T_{SS}	Internal Fixed Soft-start Time	10% V_{OUT} to 90% V_{OUT}		0.5		mS
T_{DLY}	EN Delay Time	EN High to 1st Switching Pulse		240		uS
SWITCHING FREQUENCY						
F_{SW}	Switching Frequency, CCM Operation	VIN = 5V, VOUT = 1.8V, CCM		1,500		kHz

POWER STAGE						
$R_{DSON(HS)}$	High-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 5V		200		mΩ
$R_{DSON(LS)}$	Low-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 5V		135		mΩ
T_{ON_MIN}(1)	Minimum On Pulse Width			80		nS
T_{DEAD}	Dead Time			10		nS
OVER CURRENT PROTECTION						
$I_{LS(OC)}$	Low-side Valley Current Limit	V_{IN} = 5V		1.8		A
$I_{HS(OC)}$	High-side Valley Current Limit	V_{IN} = 5V		2.5		A
$I_{LS(NOC)}$	Low-side Negative Current Limit, PJ10515F	V_{IN} = 5V`		0.8		A
OUTPUT OVP AND UVP						
$V_{IN\_OVP\_R}$	V_{IN} OVP Rising Threshold		5.95	6.05	6.15	V
$V_{IN\_OVP\_F}$	V_{IN} OVP Failing Threshold		5.6	5.7	5.8	V
$V_{IN\_OVP\_HYS}$	V_{IN} OVP Hysteresis			0.35		V
$V_{OUT\_OVP\_R}$	Output OVP Rising			116%		
$V_{OUT\_OVP\_F}$	Output OVP Falling			111%		
$V_{OUT\_UVP\_F}$	Output UVP Failing			66.7%		
$V_{OUT\_UVP\_R}$	Output UVP Rising			73%		
$T_{HCP(WAIT)}$	Wait Time before Entering UV Hiccup			90		uS
$T_{HCP(OFF)}$	UVP Hiccup Time before Re-startup			4.5		mS
OVER TEMPERATURE PROTECTION						
T_{SD}	Thermal shutdown temperature			150		°C
	Thermal shutdown hysteresis			30		°C

(1) Guaranteed by design

FEATURE DESCRIPTION

Overview

PJ10515/F operates at input supply voltage range of 2.5V to 5.5V, and supports up to 1.5A continuous output current. PJ10515/F operates with 1.5MHz switching frequency. The buck converter integrates high-side and low-side MOSFETs (HS-FET and LS-FET), adopts peak current mode (PCM) control to provide fast transient response without external loop compensation, which can help to save output capacitors and reduce solution size.

Device Operation Modes

Continuous Current Mode (CCM)

When the load current is higher than half of the peak inductor current, the converter operates in CCM. In CCM, the switching frequency is fixed and the output voltage ripple is the smallest. The device can provide a maximum continuous output current of 1.5A.

As shown in Figure-1, during CCM operation, the internal clock initiates one pulse, and the HS-FET is turned on, with the inductor current ramping up. When the inductor current reaches the COMP voltage, the HS-FET is turned off and the LS-FET is turned on, with the inductor current decreasing until the next rising edge of the clock. The switching frequency depends on the internal clock and is therefore fixed.

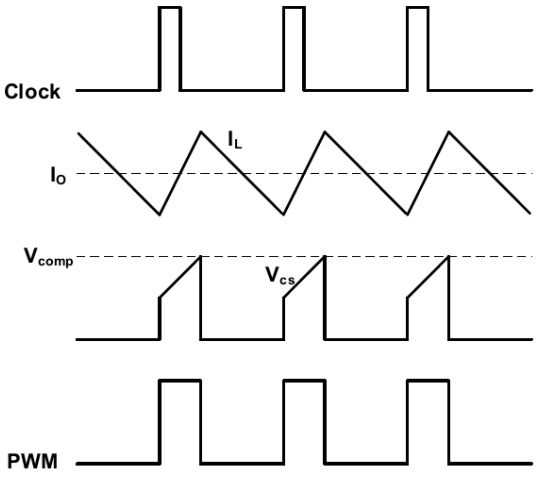


Figure-1 PCM control schema waveform

Pulse Frequency Modulation (PFM)

PJ10515 automatically enters PFM at light-load condition to maintain high efficiency. As the load current decreases, the inductor current reduces as well and eventually comes to a point that its ripple valley reaches zero level, which is the boundary between CCM and DCM. The LS-FET is turned off when the inductor crossing zero is detected. As the load current further decreases, the converter runs into DCM.

As the load current is lowered, the required peak current on each switching cycle is lessened and the COMP voltage is reduced by the error amplifier. When the COMP voltage is clamped, the switching frequency will decrease to maintain high efficiency operation.

Forced Pulse Width Modulation (FPWM)

PJ10515F operates in FPWM at light-load condition to maintain constant switching frequency and tight output voltage ripples. The LS-FET is forced on when the HS-FET is in its off state and after the dead time, until the next cycle HS-FET is turned on. This mode allows inductor current flowing from output capacitor to the switching node through LS-FET's drain-to-source terminals, which is called negative current. In this case, the switching frequency nearly keeps constant over full range of load current achieving tight output voltage ripples.

Precise Enable Control

PJ10515/F provides an EN pin, as an external IC enable control, to enable or disable the device. When the EN pin voltage rises above the rising threshold voltage ($V_{EN(R)}$) while the VIN voltage is higher than VIN under-voltage lock-out threshold ($V_{UVLO(R)}$), the device turns on. If the EN pin voltage is pulled below the falling threshold voltage ($V_{EN(F)}$), the regulator stops switching and enters the shutdown mode, that is, the regulator is disabled, and switching is inhibited even if the VIN voltage is above VIN under-voltage lock-out threshold ($V_{UVLO(R)}$). Do not leave the EN pin floating.

Soft Start and Pre-biased Soft Start

PJ10515/F provides an internal soft-start feature to ensure inrush control and smooth output voltage ramping during power-up, and the output voltage starts to rise after a 240μs delay from EN rising edge. When the IC starts, the soft-start circuitry generates a soft-start voltage (SS) ramping up from 0V. When it is below the internal reference voltage (V_{REF}), SS overrides V_{REF} so the error amplifier and comparator use SS as the reference voltage. The output voltage smoothly ramps up. Once SS rises above V_{REF}, VREF regains control. At this time the soft start process ends, and PJ10515/F enters steady state operation. The soft start time (T_{SS}) is internal fixed at around 0.5ms (10%V_{OUT} to 90%V_{OUT}).

If the output capacitor is pre-biased at startup, the PJ10515/F initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

Output UVP with Hiccup mode

PJ10515/F integrates output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (V_{UVP}), the UV comparator will go high to turn off both the internal HS-FET and LS-FET.

If the output under-voltage condition continues for a period time of $T_{HCP(WAIT)}$, PJ10515/F will enter output UVP with hiccup mode. During hiccup mode, the IC will shut down for a period time of $T_{HICCUP(OFF)}$, and then attempt to recover automatically. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. The hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then the converter resumes normal operation as soon as the over-load or short-circuit condition is removed.

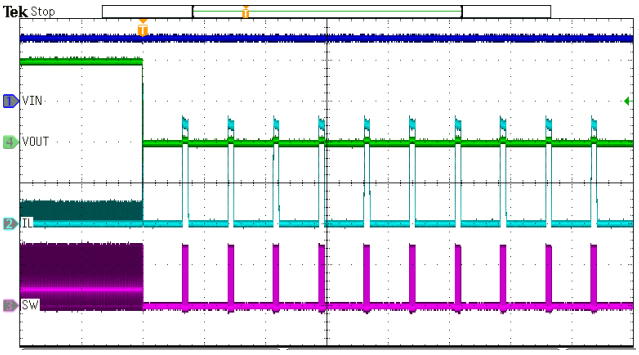


Figure-2. UVP Hiccup mode

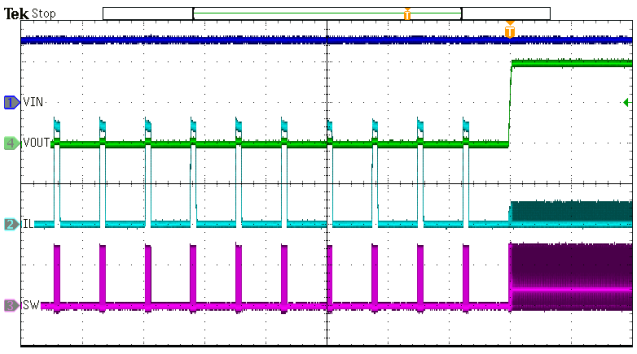


Figure-3. UVP Hiccup recovery

Peak and Valley Over-Current Limit

PJ10515/F has cycle-by-cycle peak over current limit control (OCL). During HS-FET on state, when the sensed inductor current reaches the current reference generated by the COMP voltage, HS-FET will turn off. When the over-current condition happens and the output voltage drops, the COMP voltage will bet set high. The COMP voltage has a maximum clamp internally, generating the peak current limit ($I_{HS(OC)}$), which limit the output current.

PJ10515/F also has cycle-by-cycle valley over current limit control (OCL). The inductor current is monitored during the LS-FET on state. At the end of a clock cycle, if the sensed inductor current is higher than the valley current limit ($I_{LS(OC)}$), the HS-FET will not turn on, and the LS-FET will keep on state. At the next clock cycle, if the sensed inductor current is lower than $I_{LS(OC)}$, the HS-FET will turn on.

If the output load current exceeds the available inductor current (limited between $I_{HS(OC)}$ and $I_{LS(OC)}$), the output capacitor needs to supply the extra current so that the output voltage will begin to drop. If it drops below the output under-voltage protection threshold (V_{UVP}), the IC will stop switching into UV hiccup mode to avoid excessive heat.

Negative Over-Current Limit (PJ10515F only)

PJ10515F is the part which is FPWM part and allows negative current operation. In case of FPWM operation, high negative current may be generated as an external power source is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of low-side MOSFET and compares it with negative over-current limit threshold (I_{NOC}). Once the negative current exceeds the NOC threshold, the low-side MOSFET will be turned off immediately, and then the high-side MOSFET will be turned on to discharge energy of the output inductor. This behavior can keep the valley of negative current at NOC threshold to protect LS-FET.

Output Over-Voltage Protection

PJ10515/F integrates output over-voltage protection (OVP) to minimize output voltage overshoot and protect down-stream devices when recovering from output fault conditions or strong unload transients. The OVP circuitry detects overvoltage condition by monitoring the feedback voltage (V_{FB}). When V_{FB} rises above the OVP threshold (V_{OVP}), the OVP comparator output turns high and both HS-FET and LS-FET are turned off to avoid V_{OUT} further rising higher. Once the V_{OUT} drops below V_{OVP} falling threshold, the IC starts switching again. This function is a non-latch operation.

Input Over-Voltage Protection

PJ10515/F integrates input over voltage protection (OVP). The OVP circuitry detects over-voltage condition by monitoring the input voltage (V_{IN}). When V_{IN} rises above the OVP threshold ($V_{IN(OVP)}$), the OVP comparator output turns high and both HS-FET and LS-FET are turned off, the device stops working. Once V_{IN} drops below $V_{IN(OVP)}$ falling threshold, the IC starts switching again. This function can ensure the reliability when the input voltage is unstable with overvoltage spike.

Over Temperature Protection

PJ10515/F includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold ($T_{J(SD)}$). Once the junction temperature cools down by a thermal shutdown hysteresis ($T_{J(HYS)}$), the IC will resume normal operation with a complete soft start.

APPLICATION INFORMATION

Overview

The output stage of synchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained. This section describes the detailed design process based on one design example.

Output Voltage Setting

As shown in Figure-4, PJ10515/F can be set to different output voltages by using an external voltage resistor divider connected to the FB pin.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB(T)}}{R_{FB(B)}}\right)$$

where V_{REF} = 0.6V

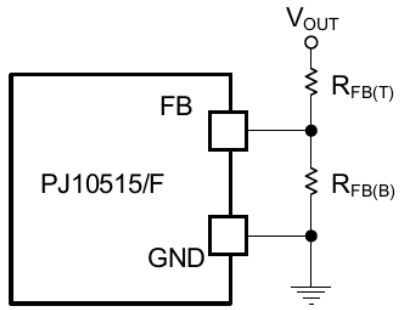


Figure-4. Output voltage setting

It is recommended to design from the bottom side feedback resistor $R_{FB(B)}$. Too large $R_{FB(B)}$ will make the FB pin more susceptible to external noises, while too small $R_{FB(B)}$ will increase the power loss of the resistor divider. $R_{FB(B)}$ = 10kΩ~50kΩ is recommended. And the top side feedback resistor $R_{FB(T)}$ can be calculated by the following formula :

$$R_{FB(T)} = R_{FB(B)} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} = 0.6V

For example, in the application with 1.8V output voltage, choose $R_{FB(B)}$ as 10kΩ and then $R_{FB(T)}$ is calculated as 20kΩ.

In the application scenarios where higher precision of output voltage is required, it is recommended to select a voltage resistor divider with a precision of 1% or even higher.

Output Inductor Selection

The selection of inductor is related to the size, cost, efficiency, and transient response performance. Three key parameters of inductor are mainly considered: inductance (L), saturation current (I_{SAT}) and inductor DC resistance (DCR).

To compromise the volume and power consumption of the inductor, it is recommended to select an inductor whose current ripple (ΔI_L) is 20%-50% of the rated current (I_{rated}) of PJ10515/F, as shown in the following formula :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{rated} \times K_L}$$

where

V_{IN} is input voltage,

V_{OUT} is output voltage,

f_{SW} is switching frequency,

I_{rated} is the rated current of PJ10515/F : 1.5A

K_L is 20%-50%

Once the inductor has been selected according to the above formula, the actual inductor current ripple ΔI_L

and peak current ($I_{L(peak)}$) can be obtained by the following formula :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where

$I_{OUT(MAX)}$ is maximum output current

The inductor whose saturation current I_{SAT} is at least greater than the peak current $I_{L(peak)}$ should be selected with a some margin (for example, 10%) to ensure that the inductor will not be saturated during normal steady-state operation of the chip.

Output Capacitor Selection

The selection of output capacitor is related to the output voltage ripple, load transient performance and loop stability.

Output voltage ripple V_{RIPPLE} consists of two main parts. One is the resistive ripple $V_{RIPPLE(ESR)}$ generated by the inductive current at the equivalent series resistance ESR of the output capacitor. The other part is capacitive ripple $V_{RIPPLE(C)}$ generated by charging and discharging the output capacitor with the inductance ripple current. The calculation formula is as follows :

$$V_{RIPPLE} = \sqrt{V_{RIPPLE(ESR)}^2 + V_{RIPPLE(C)}^2}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times ESR$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{sw}}$$

The actual ripple can be simply estimated as :

$$V_{RIPPLE} > Max\left(V_{RIPPLE(ESR)}, V_{RIPPLE(C)}\right)$$
$$V_{RIPPLE} < V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

Input Capacitor Selection

Since the input current of Buck converter is pulsed discontinuous current, it is recommended to use ceramic capacitors at the input to provide pulsed input current to keep the DC input voltage stable. The input voltage ripple can be calculated by the following formula :

$$V_{IN(Ripple)} \approx D \times I_{OUT} \times \frac{1 - D}{C_{IN} \times f_{sw}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN}}$$

In addition, since the input capacitor is pulsed discontinuous current, the selected input capacitor must be able to withstand large AC RMS current :

$$I_{IN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D(1 - D)}$$

In addition, to optimize the EMI performance and ensure the reliable and stable operation of the chip, besides using the ceramic capacitor as the input capacitor CIN, it is recommended to add another 0.1μF ceramic capacitor (0603/0402 package) to the VIN and GND pins as close as possible. It is important to note that although the ceramic capacitor has excellent high-frequency performance and stable lifetime, but due to the low ESR characteristics of ceramic capacitor, the actual input voltage may start ringing in some input hot-plug scenarios, and the worst input voltage even may ring to 2 times nominal voltage, thus this over-voltage ringing may breakdown IC. In this case, it is recommended to add an additional electrolytic capacitor with large ESR in parallel at the input voltage end or to add a TVS diode to limit or clamp the input over-voltage ringing.

The recommended component selection is shown in Table -1.

Table-1. Recommended Component Selection Table

V_{OUT} (V)	$R_{FB(T)}$ (kΩ)	$R_{FB(B)}$ (kΩ)	L_{typ} (μH)	C_{IN}	C_{OUT}
3.3	45	10	1.2	10μF+100nF	22μF
2.5	31.7	10	1.2	10μF+100nF	22μF
1.8	20	10	1.2	10μF+100nF	22μF
1.2	10	10	1.2	10μF+100nF	22μF
1.05	7.5	10	1.2	10μF+100nF	44μF

Feedforward Capacitor Selection

PJ10515/F integrates internal loop compensation, which can simplify the external circuit design and achieve fast load transient response performance. In some applications where the load transient response is more demanding, the transient response performance can be further improved by adding feedforward resistor R_{FF} and capacitor C_{FF} across the top FB divider resistor. In consideration of noise coupling, it is recommended to use R_{FF}= 2kΩ~10kΩ, and do not use C_{FF} higher than 47pF. Note that the actual R_{FF} and C_{FF} are optional devices, and it is recommended to optimize the selection through bench checks of load transient response and load regulation performance.

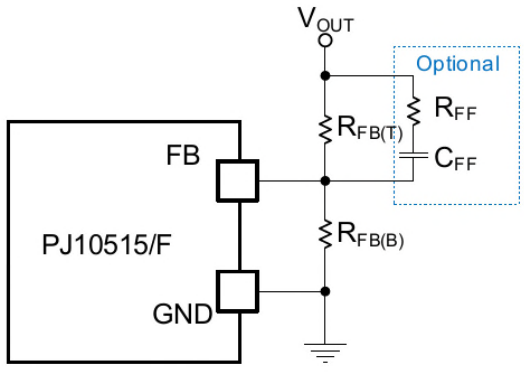


Figure-5. Feedforward Resistor and Capacitor

PCB Design Guidelines

PCB design is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place the input ceramic capacitor as close to VIN and GND pins as possible.

2. The trace of the main power loop CIN→L→COUT→GND should be as short and wide as possible to reduce trace voltage drop and improve conversion efficiency.

3. The SW node voltage is high frequency square wave. Appropriately reducing the size of SW node can improve EMI performance; On the other hand, appropriately increasing the size of SW node can optimize heat dissipation performance. Take appropriate compromise according to the actual situation is recommended.

4. The FB trace should be as far away from noise sources as possible, such as SW node.

5. The sampling point of the output voltage VOUT should be placed near the end of the output capacitors and place the voltage divider resistors near the FB pin.

6. The trace and copper of VIN and GND node should be as wide as possible to help heat dissipation. In multilayer PCB designs, it is recommended to leave a complete GND layer for the GND node and to add enough vias between the GND layer and the chip layer. The vias can optimize heat dissipation performance.

Typical Reference Design

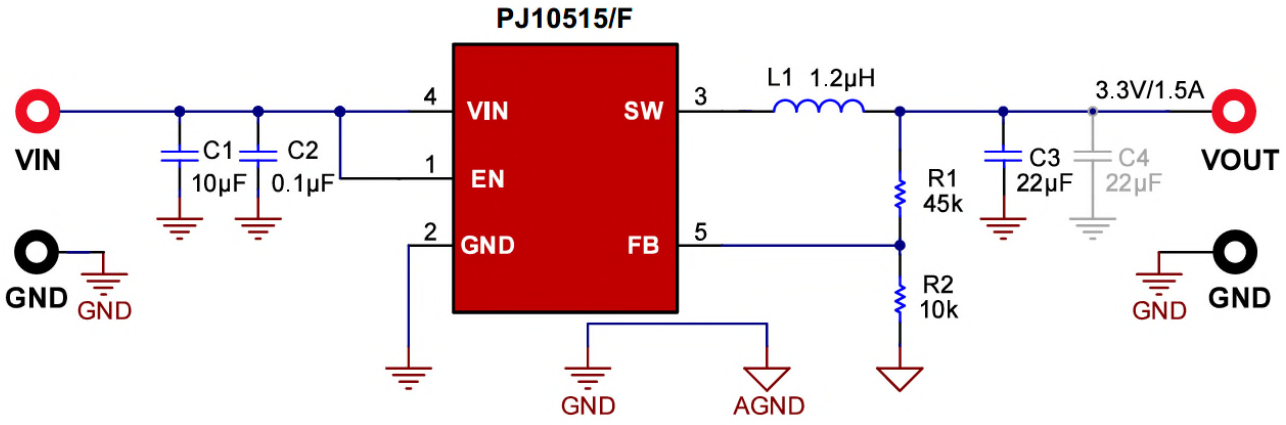


Figure-6. V_{IN}= 5V, V_{OUT}= 3.3V, I_{OUT}= 1.5A

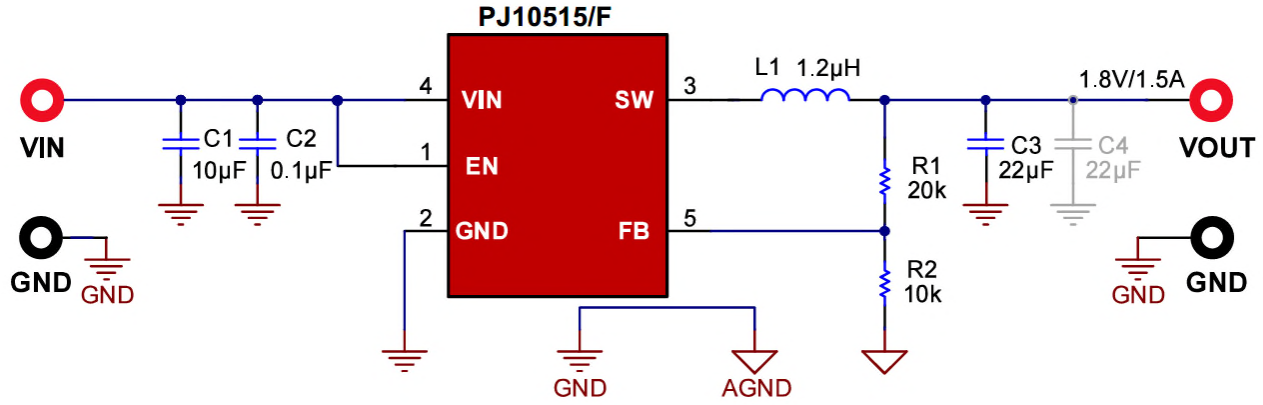


Figure-7. V_{IN}= 5V, V_{OUT}= 1.8V, I_{OUT}= 1.5A

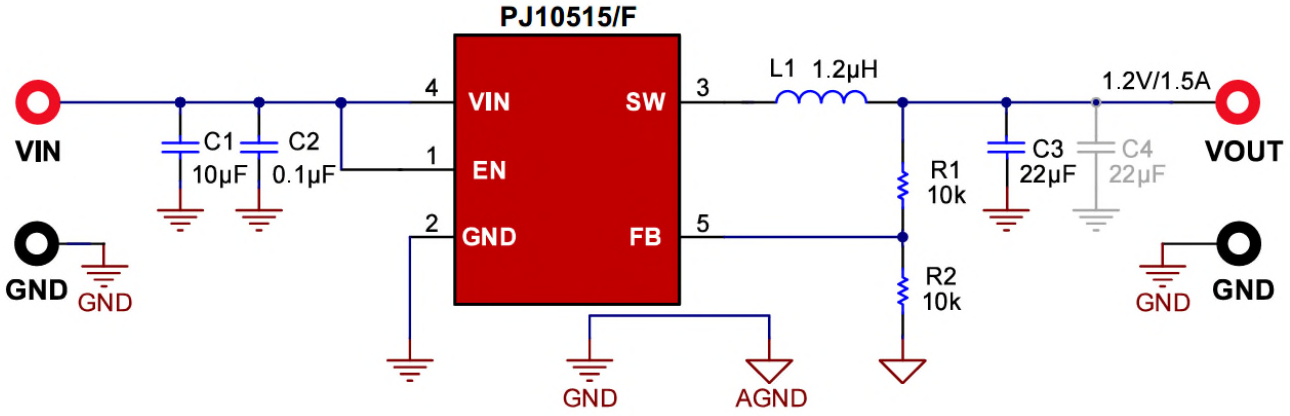


Figure-8. V_{IN}= 5V, V_{OUT}= 1.2V, I_{OUT}= 1.5A

Typical Operating Characteristics

Test Conditions: V_{IN} = 5V, V_{OUT} = 1.8V, T_A = 25°C (unless otherwise noted)

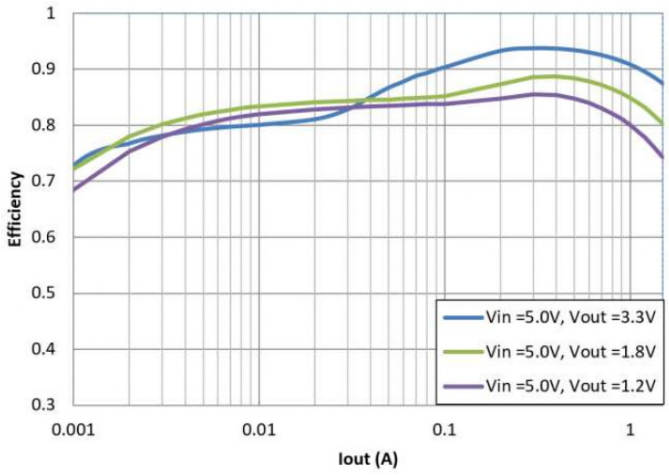


Figure-9. PJ10515/F V_{IN} = 5V Efficiency

L = 1.5μH, DCR = 12.1mΩ

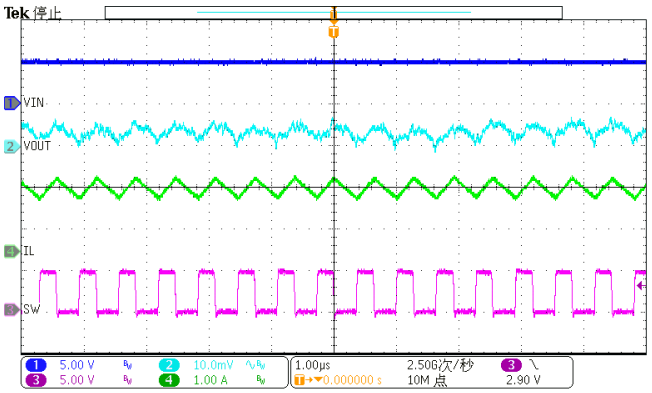


Figure-10. Steady State, I_{OUT} = 1.5A

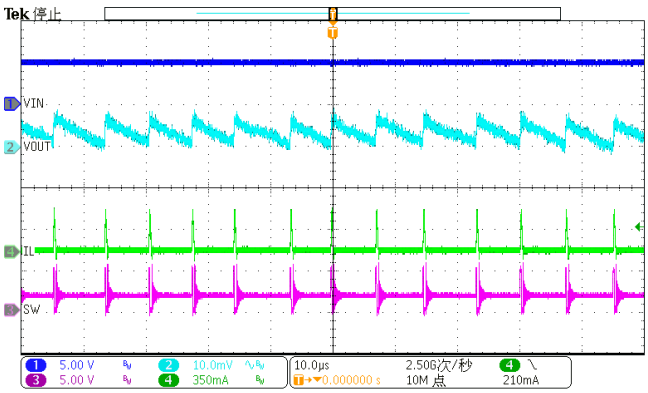


Figure-11. Steady State, I_{OUT} = 10mA

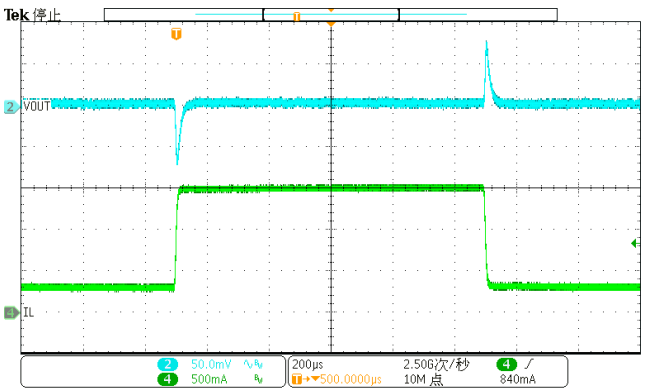


Figure-12. Load Transient

I_{OUT} = 0.3A-1.5A, 250mA/μs

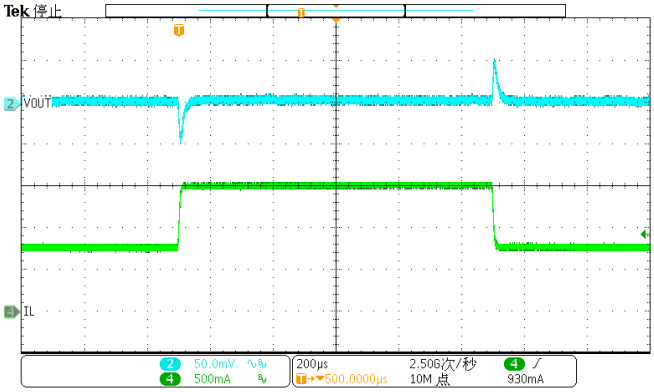
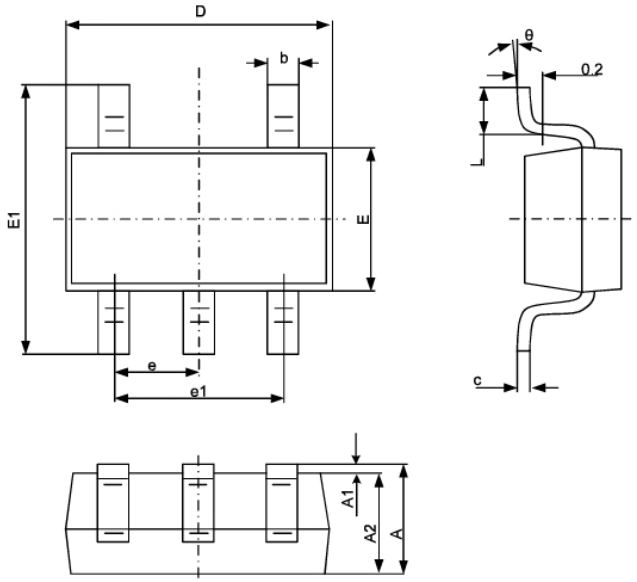


Figure-13. Load Transient

I_{OUT} = 0.75A-1.5A, 250mA/μs

PACKAGE DIMENSION

SOT23-5



Symbol	Dimensions (Millimeters)		Dimensions (Inches)	
	Min.	Max.	Min.	Max.
A	-	1.350	0.035	0.047
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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