PJ67250

2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager In a QFN4x4-32 Package

GENERAL DESCRIPTION

The PJ67250 device, incorporating patented accurately measures technology, is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the PJ67250 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v3.1 compatible interface.

The PJ67250 device supports TURBO mode 3.0 by providing the available max power and max current to the host system. The device also supports Battery Trip Point to send a BTP interrupt signal to the host system at the pre-set state of charge thresholds.

The PJ67250 provides software-based 1st- and 2nd-level safety protection against over-voltage, under-voltage, overcurrent, short-circuit current, overload, and over-temperature conditions, as well as other pack- and cell- related faults.

SHA-1/SHA-256 and ECC authentication, with secure memory for authentication keys, enables identification of genuine battery packs.

The compact 32-lead QFN package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

FEATURES

- Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Patented Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
- High Side N-CH Protection FET Drive
- Integrated Cell Balancing While Charging or at Rest
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
  - Charge Timeout
  - CHG/DSG FETs
  - AFE
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
  - Cell Balancing
- Supports TURBO Mode 3.0
- Supports Battery Trip Point (BTP)
- Diagnostic Lifetime Data Monitor and Black Box Recorder
- LED Display
- Supports Two-Wire SMBus v3.1 Interface
- SHA-1/SHA-256, ECC Authentication
- Compact Package: 32-Lead QFN4x4

APPLICATIONS

- Notebook / Tablets
- UPS and Battery Backup System
- Power Tools and Clean Robot
- Drone

ORDERING INFORMATION

ORDER NUMBER	Marking ID	Package	Description
PJ67250QW_R1	A1 YM DNN	QFN4x4-32	Halogen Free in T&R, 3000 pcs/Reel

SIMPLE SCHEMATIC

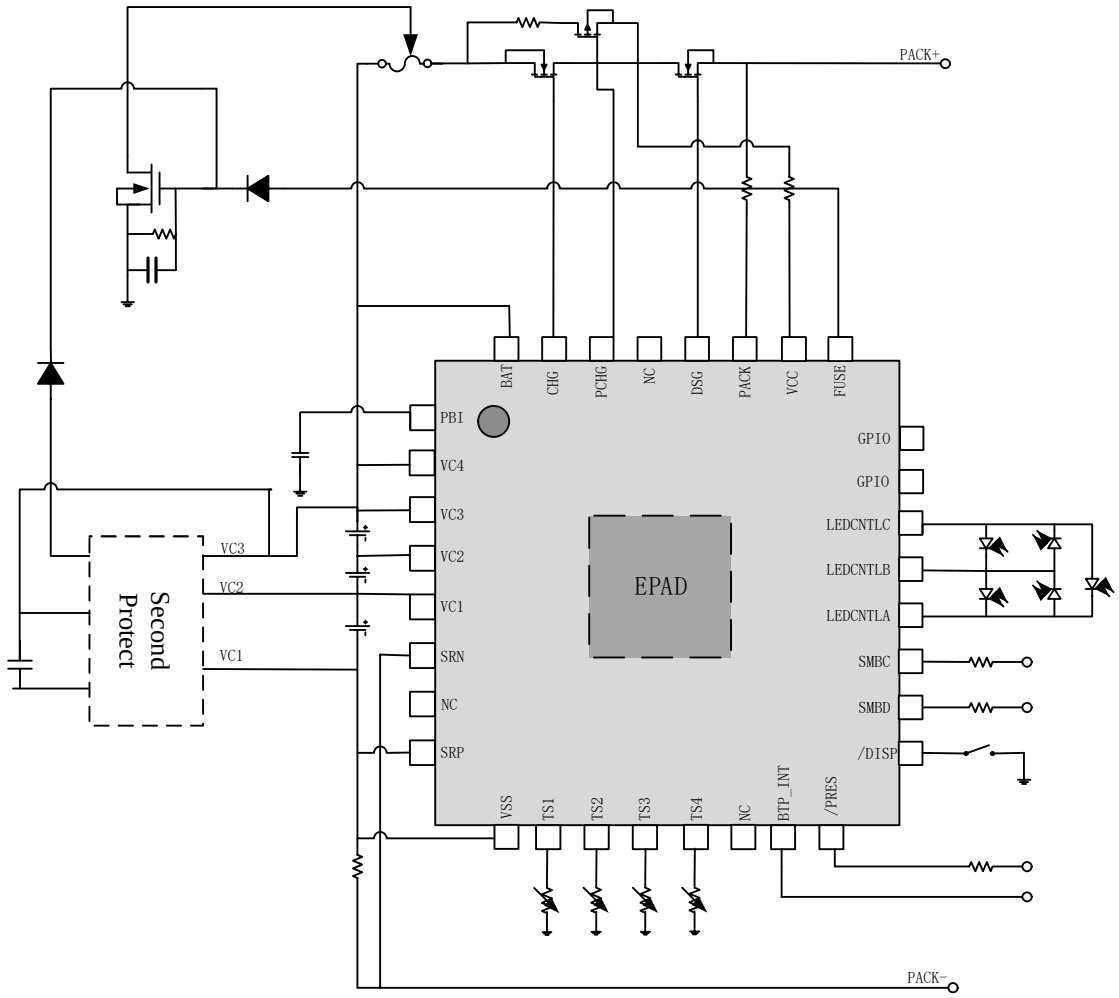
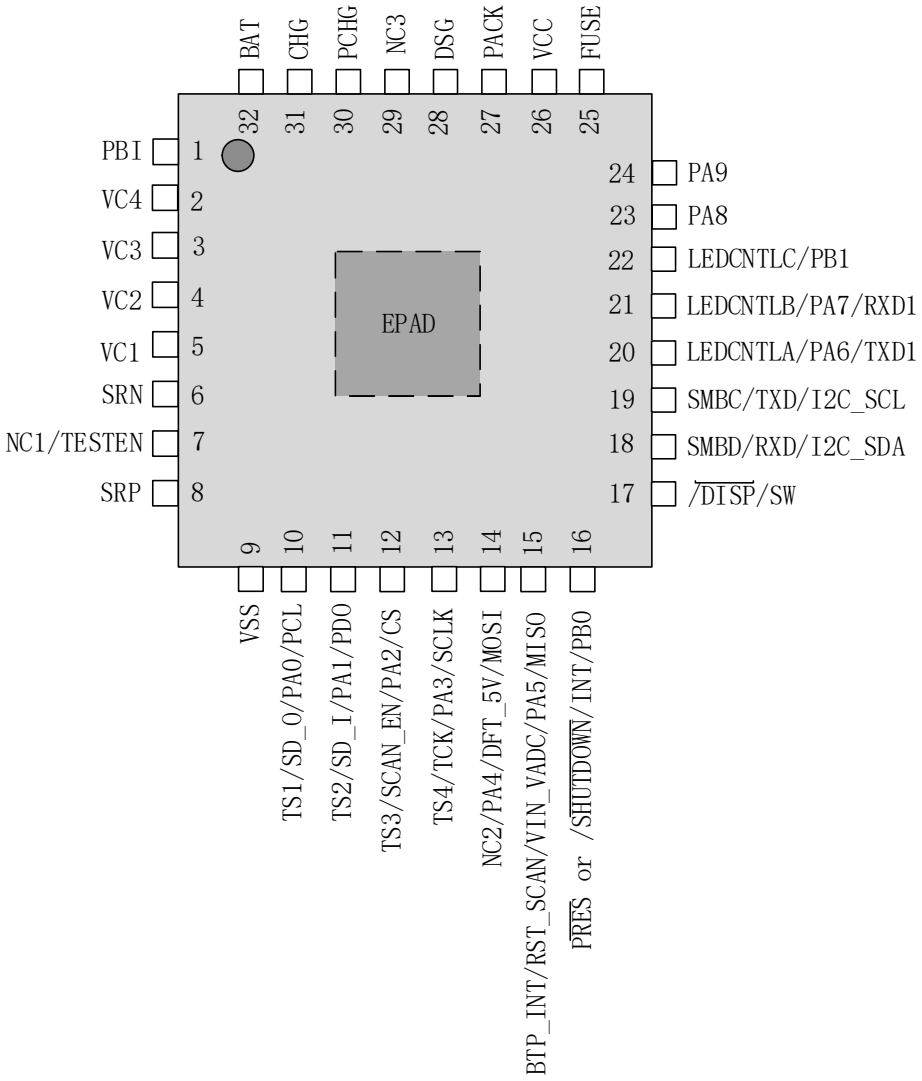


Figure-1. PJ67250 Simple Schematic

PIN CONFIGURATION

(TOP VIEW)



FUNCTIONAL PIN DESCRIPTION

TERMINAL		PIN TYPE	DESCRIPTION
NUMBER	NAME		
1	PBI	P	Power supply backup input pin
2	VC4	I	Sense voltage input pin for most positive cell, and balance current input for most positive cell
3	VC3	I	Sense voltage input pin for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell
4	VC2	I	Sense voltage input pin for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell
5	VC1	I	Sense voltage input pin for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell
6	SRN	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor
7	NC1	-	Not internally connected, it can connect to ground
	TESTEN	I	TESTEN pin for DFT
8	SRP	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor
9	VSS	P	Device Ground
10	TS1	I	Temperature sensor 1 thermistor input pin
	SD_0	I/O	SD_0 pin of DFT
	PA0	I/O	General purpose GPIO
	PCL	I/O	PCL pin of SWD
11	TS2	I	Temperature sensor 2 thermistor input pin
	SD_I	I/O	SD_I pin of DFT
	PA1	I/O	General purpose GPIO
	PDO	I/O	PDO pin of SWD
12	TS3	I	Temperature sensor 3 thermistor input pin
	SCAN_EN	I	SCAN_EN pin of DFT
	PA2	I/O	General purpose GPIO
	CS	I	Chip Select pin of SPI, pull it high , when it was selected

TERMINAL		PIN TYPE	DESCRIPTION
NUMBER	NAME		
13	TS4	I	Temperature sensor 4 thermistor input pin
	TCK	I	TCK pin of DFT
	PA3	I/O	General purpose GPIO
	SCLK	I	Clock pin of SPI
14	NC2	-	Not internally connected
	DFT_5V	I	Enable pin of DFT_5V
	PA4	I/O	General purpose GPIO
	MOSI	O	Host data output, slave data input signal
15	BTP_INT	O	Power Ground. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias
	RST_SCAN	I	Reset scan pin of DFT
	VIN_VADC	I	VADC input
	SP5	I/O	General purpose GPIO
	MISO	I	The host data input, slave data output signal
16	/PRES or /SHUTDN	O	Current monitor output
	PB0	I/O	General purpose GPIO
	INT	O	Interrupt output of AFE
17	DISP	-	EN input. Apply logic high to enable the chip
	SW	O	Interrupt wakes up the chip from Shutdown
18	SMBD	I/O	SMBus data pin
	RXD	I/O	Receiver terminal of UART
	I2C_SDA	I	Data input of I2C interface
19	SMBC	I/O	SMBus clock pin
	TXD	I/O	Transmitter terminal of UART
	I2C_SCL	I	Clock input of I2C

TERMINAL		PIN TYPE	DESCRIPTION
NUMBER	NAME		
20	LEDCNTLA	I/O	LED display control pin
	PA6	I/O	General purpose GPIO
	TXD1	I/O	Transmitter1 terminal of UART
21	LEDCNTLB	I/O	LED display control pin
	PA7	I/O	General purpose GPIO
	RXD1	I/O	Receiver1 terminal of UART
22	LEDCNTLC	I/O	LED display control pin
	PB1	I/O	General purpose GPIO
23	PA8	I/O	PTC, Safety PTC thermistor input pin. To disable, connect both PTC and PTCEN to VSS
24	PA9	I/O	PTCEN, Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect both PTC and PTCEN to VSS
25	FUSE	O	Fuse drive output pin
26	VCC	P	Secondary power supply input
27	PACK	I	Pack sense input pin
28	DSG	O	NMOS Discharge FET drive output pin
29	NC3	-	Not internally connected
30	PCHG	O	PMOS Precharge FET drive output pin
31	CHG	O	NMOS Charge FET drive output pin
32	BAT	P	Primary power supply input pin

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	BAT, VCC, PBI	-0.3	30	V
	PACK, PA6, PA7, PA8, PA9, PB1	-0.3	30	V
	PA0, PA1, PA2, PA3, PA4, PA5, PB0, SW, TESTEN	-0.3	3.6	V
	SRP, SRN	-0.3	3.5	V
	VC4	VC3 - 0.3	VC3 + 8.5 VSS + 30	V
	VC3	VC2 - 0.3	VC2 + 8.5 VSS + 30	V
	VC2	VC1 - 0.3	VC1 + 8.5 VSS + 30	V
	VC1	VSS - 0.3	VSS + 8.5 VSS + 30	V
	CHG, DSG, VBMC	-0.3	32	V
	PCHG, SDSG	-0.3	30	V
Current Range	VSS source Current		50	mA
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3), all pins	-1	1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	BAT, VCC, PBI	4.4		26	V
$V_{SHUTDOWN-}$	Shutdown voltage	VPACK < VSHUTDOWN-	1.75	2.2	2.6	V
$V_{SHUTDOWN+}$	Start-up voltage	VPACK > VSHUTDOWN- + VHYS	2.05	2.45	2.85	V
V_{HYS}	Shutdown voltage hysteresis	VSHUTDOWN+ - VSHUTDOWN-		250		mV
V_{IN}	Input voltage range	PACK, SMBC, SMBD, PRES, BTP_IN, DISP			26	V
		TS1, TS2, TS3, TS4			V_{REG}	
		LEDCNTLA, LEDCNTLB, LEDCNTLC			V_{BAT}	
		SRP, SRN	-0.2		0.2	
		VC4	V_{VC3}		V_{VC3} +5	
		VC3	V_{VC2}		V_{VC2} +5	
		VC2	V_{VC1}		V_{VC1} +5	
		VC1	V_{VSS}		V_{VSS} +5	
V_O	Output voltage range	CHG, DSG, PCHG, FUSE			26	V
C_{PBI}	External PBI capacitor		2.2			uF
T_{OPR}	Operating temperature		-40		85	°C

THERMAL INFORMATION

THERMAL RESISTANCE		WQFN-32 (4mm x 4mm)	UNIT
Θ_{JA}(1)	Junction to ambient thermal resistance (JESD51-7)	46.8	°C/W
$\Theta_{JC(top)}$	Junction to case (top) thermal resistance	19.5	°C/W
Θ_{JB}	Junction to board thermal resistance	14.7	°C/W
ψ_{JT}	Junction to top characterization parameter	0.8	°C/W
ψ_{JB}	Junction to board characterization parameter	14.4	°C/W
$\Theta_{JC(bottom)}$	Junction to case (bottom) thermal resistance	3.8	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 85°C, V_{IN} = 14.4V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY Current - V_{CC} = 4.4V to 26V						
I_{NORMAL}	NORMAL mode	CHG on. DSG on, no Flash write		400	600	uA
I_{SLEEP}	SLEEP mode	CHG off, DSG on, no SMBus (5S/ test)		80	120	uA
		CHG off, DSG on, no SMBus (3S/ test)		88	132	uA
		CHG off, DSG off, no SMBus (5S/ test)		52	78	uA
$I_{SHUTDOWN}$	SHUTDOWN mode	When T_J = 85°C, <10uA		7	10	uA
Power Supply Control - V_{CC} = 4.4V to 26V						
$V_{SWITCHOVER-}$	BAT to Vcc switchover voltage	$V_{BUS} > V_{SWITCHOVER-}$	2.6	3.1	3.6	V
$V_{SWITCHOVER+}$	Vcc to BAT switchover voltage	$V_{BUS} < V_{SWITCHOVER-} + V_{HYS}$	2.25	2.85	3.4	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} - V_{SWITCHOVER-}$		250		mV
AFE Power-On Reset - V_{CC} = 4.4V to 26V						
V_{REG}	AFE Voltage	V_{REG}	1.95	2	2.05	V
V_{REGIT-}	Negative-going voltage input	V_{REG}	1.7	1.8	1.9	V
V_{HYS}	Power-on reset hysteresis	VREGIT+ – VREGIT–	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	uS
AFE Watchdog Reset and Wake Timer - V_{CC} = 4.4V to 26V						
t_{WDT}	AFE watchdog timeout	t_{WDT} = 500	372	500	628	mS
		t_{WDT} = 1000	744	1,000	1256	
		t_{WDT} = 2000	1,488	2,000	2,512	
		t_{WDT} = 4000	2,976	4,000	5,024	
t_{WAKE}	AFE wake timer	t_{WAKE} = 250	186	250	314	mS
		t_{WAKE} = 500	372	500	628	
		t_{WAKE} = 1000	744	1,000	1,256	
		t_{WAKE} = 2000	1,488	2,000	2,512	
t_{FETOFF}	FET off delay after reset	t_{FETOFF} = 512	409	512	614	mS
Current Wake Comparator - V_{CC} = 4.4V to 26V						
V_{WAKE}	Wake voltage threshold	V_{WAKE} = ±0.625 mV	±0.3	±0.625	±0.9	mV
		V_{WAKE} = ±1.25 mV	±0.6	±1.25	±1.8	
		V_{WAKE} = ±2.5 mV	±1.2	±2.5	±3.6	
		V_{WAKE} = ±5 mV	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		°C
t_{WAKE}	Time from application of current to wake interrupt				700	µS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE(SU)}$	Wake comparator startup time		500	1,000		µS
VC1, VC2, VC3, VC4, BAT, PACK - V_{CC} = 4.4V to 26V						
K	Scaling factor	VC1 - VSS, VC2 - VC1, VC3 - VC2, VC4 - VC3	0.198	0.2	0.202	—
		BAT - VSS, PACK - VSS	0.049	0.05	0.051	
		VREF2	0.49	0.5	0.51	
V_{IN}	Input voltage range	VC1 - VSS, VC2 - VC1, VC3 - VC2, VC4 - VC3	- 0.2		5	V
		BAT - VSS, PACK - VSS	- 0.2		20	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4 cell balancing off, cell detach detection off, ADC multiplexer off			1	µA
I_{CB}	Internal cell balance current	IDS(ON) internal switching current, when 2V < V_{DS} < 4 V	2		20	mA
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8 V	30	50	70	µA
HV GPIO (PA1) - V_{CC} = 4.4V to 26V						
V_{OH}	Output voltage high	I_{OH} = 1.5 mA	3			V
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	Pulldown resistance	V_{DD}=3.3V	42	60	78	KΩ
HV GPIO SMBus - V_{CC} = 4.4V to 26V						
V_{IH}	Input voltage high (SMBus,I2C)	V_{REG} = 1.8 V	1.26			V
		V_{REG} = 1.2 V	0.96			V
	Input voltage high (UART)	V_{DD} = 3.3V	0.7xV_{DD}			V
V_{IL}	Input voltage Low (SMBus,I2C)	V_{REG} = 1.8 V			0.54	V
		V_{REG} = 1.2 V			0.4	V
	Input voltage Low (UART)	V_{DD} = 3.3V			0.3xV_{DD}	V
V_{OH}	Output voltage high	I_{OH}= 3mA	3			V
V_{OL}	Output voltage low	I_{OL}= 3mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PH}	Pull-up resistance	V_{DD} = 3.3V	48	60	72	KΩ
R_{PD}	Pull-down resistance	V_{DD} = 3.3V	42	60	78	KΩ
GPIO (PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PB0, SW) - V_{CC} = 4.4V to 26V						
V_{IH}	Input voltage high	V_{DD}=3.3V	0.7xV_{DD}			V
V_{IL}	Input voltage low				0.3xV_{DD}	V
V_{OH}	Output voltage high	Input voltage high	3			V
V_{OL}	Output voltage low	IOL=1.5mA			0.4	V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PH}	Pull-up resistance	V_{DD} = 3.3V	48	60	72	KΩ
R_{PD}	Pull-down resistance	V_{DD} = 3.3V	42	60	78	KΩ
LED Display - V_{CC} = 4.4V to 26V						
V_{IH}	Input voltage high		1.45			V
V_{IL}	Input voltage low				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 3.0 V, I_{OH} = –22.5 mA	V_{BAT}-1.6			V
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
I_{SC}	High level output current protection		–30	–45	–60	mA
I_{OL}	Low level output current	V_{BAT} > 3.6 V, V_{OH} = 0.4 V	15.75	22.5	29.25	mA
$I_{LEDCNTLX}$	Current matching between LEDCNTLx	V_{BAT}>3.6 V		±1		%
C_{IN}	Input capacitance			20		pF
I_{LKG}	Input leakage current				1	µA
$f_{LEDCNTLx}$	Frequency of LED pattern			124		Hz
Coulomb Counter - V_{CC} = 4.4V to 26V						
Input voltage range			- 0.1		0.1	V
Full scale range			V_{REF1}/10		V_{REF1}/10	V
Integral nonlinearity		16-bit, best fit over input voltage range	±5.2		±22.3	LSB
Offset error		16-bit, Post-calibration		±2.5	±5	µV
Offset error drift		16-bit + sign, Post-calibration		0.2	0.3	µV/°C
Gain error		16-bit + sign, over input voltage range		±0.2%	±0.8%	FSR
Gain error drift		16-bit + sign, over input voltage range		30	150	PPM/°C
Effective input resistance			2.5			MΩ
Conversion time		Single conversion		250		mS
Effective resolution		Single conversion	16			Bits
VADC - V_{CC} = 4.4V to 26V						
Input voltage range		Internal reference (V_{REF1})	–0.2		1	V
		External reference (V_{REG})	–0.2		0.8 × V_{REG}	
Full scale range		V_{FS} = V_{REF1} or V_{REG}	$–V_{FS}$		V_{FS}	V
Integral nonlinearity		16-bit, Input Range -0.1 V~0.8 × V_{REF1}			±6.6	LSB
		16-bit, Input Range -0.2 V ~ -0.1 V			±13.1	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset error		16-bit, Post-calibration, $V_{FS} = V_{REF1}$		±67	±157	µV
Offset error drift		16-bit, Post-calibration, $V_{FS} = V_{REF1}$		0.6	3	µV/°C
Gain error		16-bit, –0.1 V to 0.8 × V_{FS}		±0.2%	±0.8%	FSR
Gain error drift		16-bit, –0.1 V to 0.8 × V_{FS}			30	PPM/°C
Effective input resistance			8			MΩ
Conversion time		Single conversion		31.25		mS
		Single conversion		15.63		
		Single conversion		7.81		
		Single conversion		1.95		
Resolution		No missing codes	16			Bits
Effective resolution		With sign, t_{CONV} = 31.25mS	15	16		Bits
		With sign, t_{CONV} = 15.63mS	14	15		
		With sign, t_{CONV} = 7.81mS	12	13		
		With sign, t_{CONV} = 1.95mS	10	11		
CHG, DSG FET Drive - V_{CC} = 4.4V to 26V						
Output voltage ratio		$Ratio_{CHG} = (V_{CHG} - V_{BAT}) / V_{BAT}$, 4.4V < V_{BAT} < 4.8V , 10 MΩ between BAT and CHG		2.333		—
		$Ratio_{DSG} = (V_{DSG} - V_{BAT}) / V_{BAT}$, 4.4V < V_{BAT} < 4.8V, 10 MΩ between PACK and DSG		2.333		—
		$Ratio_{VBMC} = (V_{BMC} - V_{BAT}) / V_{BAT}$, 4.4V < V_{BAT} < 4.8V , 10 MΩ between PACK and BMC		2.333		—
$V_{(FETON)}$	Output voltage, CHG and DSG on	$Ratio_{CHG} = V_{CHG} - V_{BAT}$, 4.8 < V_{BAT} , 10 MΩ between BAT and CHG	9	11	12.5	V
		$Ratio_{DSG} = V_{DSG} - V_{BAT}$, 4.8 < V_{BAT} , 10 MΩ between PACK and DSG	9	11	12.5	V
		$RatioV_{BMC} = V_{BMC} - V_{BAT}$, 4.8 < V_{BAT}, 10 MΩ between PACK and BMC	9	11	12.5	V
$V_{(FETOFF)}$	Output voltage, CHG and DSG off	$V_{DSG(OFF)} = V_{DSG} - V_{PACK}$, 10 MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)} = V_{CHG} - V_{BAT,}$ 10 MΩ between PACK and BMC	–0.4		0.4	V
		$V_{BMC(OFF)} = V_{BMC} - V_{BUS}$, 10 MΩ between PACK and BMC	–0.4		0.4	V
$R_{SHUTDOWN}$	Shut-down impedance	Shut-down Impedance of CHG MOS / DSG MOS / VBUS MOS			50	KΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L =4.7 nF between DSG and PACK, 5.1kΩ between DSG and C_L, 10 MΩ between PACK and DSG		250	500	µS
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L =4.7 nF between CHG and BAT, 5.1kΩ between CHG and C_L, 10 MΩ between PACK and CHG		250	500	
		V_{BMC} from 0% to 35% $V_{BMC(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L =4.7nF between V_{BMC} and V_{BUS}, 5.1kΩ between V_{BMC} and C_L, 10MΩ between V_{BUS} and V_{BMC}		250	500	
t_F	Fall Time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		120	250	µS
		V_{BMC} from $V_{BMC(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7nF between V_{BMC} and V_{BUS}, 5.1 kΩ between V_{BMC} and C_L, 10 MΩ between V_{BMC} and V_{BUS}		120	250	µS
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L =4.7 nF between CHG and BAT, 5.1kΩ between CHG and C_L, 10 MΩ between PACK and CHG		90	150	µS
		V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L =4.7 nF between DSG and PACK, 5.1kΩ between DSG and C_L, 10 MΩ between PACK and DSG		60	100	µS
		VBMC from VBMC(ON)(TYP) to 1 V, VBAT ≥ 2.2 V, C_L =4.7nF between V_{BMC} and V_{BUS}, 5.1kΩ between V_{BMC} and C_L, 10MΩ between V_{BUS} and V_{BMC}		60	100	µS
		VCHG from VCHG(ON)(TYP) to 1 V, VBAT ≥ 2.2 V, C_L = 27 nF between CHG and BAT, 250Ω between CHG and C_L, 10 MΩ between BAT and CHG		40	100	µS

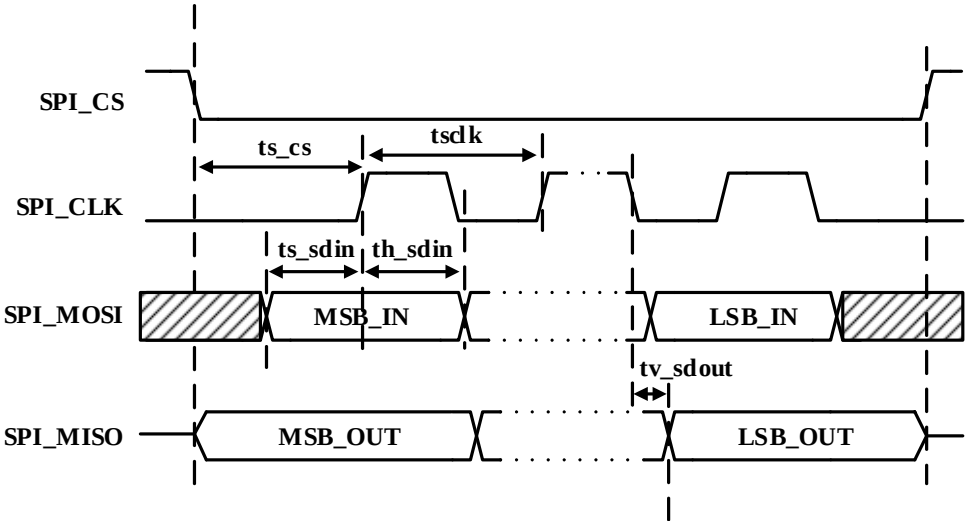
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PCHG FET Drive - V_{CC} = 4.4V to 26V						
$V_{(FETON)}$	Output voltage, P_{CHG} on	$V_{PCHG(ON)} = V_{VCC} – V_{PCHG}$, 100 KΩ between V_{CC} and PCHG	6	7	8	V
$V_{(FETOFF)}$	Output voltage, P_{CHG} off	$V_{PCHG(OFF)} = V_{VCC} – V_{PCHG}$, 100 KΩ between V_{CC} and PCHG	–0.4		0.4	V
t_R	Rise Time	V_{PCHG} from 10% to 90% $V_{PCHG(ON)(TYP)}$, V_{CC} ≥ 8 V, C_L =4.7 nF between PCHG and V_{CC}, 5.1kΩ between PCHG and C_L, 100 kΩ between CHG and V_{CC}		40	200	µS
t_F	Fall Time	V_{PCHG} from 90% to 10% $V_{PCHG(ON)(TYP)}$, V_{CC} ≥ 8 V, C_L =4.7 nF between PCHG and V_{CC}, 5.1kΩ between PCHG and C_L, 100 kΩ between CHG and V_{CC}		40	200	µS
FUSE Drive - V_{CC} = 4.4V to 26V						
V_{OH}	Output voltage high	VBAT ≥ 8 V, CL = 1 nF, IAFESDSG = 0 µA	6	7.5	8.65	V
		VBAT < 8 V, CL = 1 nF, IAFESDSG = 0 µA	V_{BAT}–0.1		V_{BAT}	V
V_{IH}	Input voltage high		1.5	2	2.5	V
$I_{AFESDSG(PU)}$	Internal pullup current	VBAT ≥ 8 V, VAFESDSG = VSS		150	330	nA
I_{DN}	Internal pullup current		41	51	61	kΩ
$R_{AFESDSG}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trip detection delay		128		256	µS
t_{RISE}	Fuse output rise time	VBAT ≥ 8 V, CL = 1 nF, VOH = 0 V to 5 V		5	20	µS
Internal Temperature Sensor - V_{CC} = 4.4V to 26V						
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9	–2.0	–2.1	mV/°C
		$V_{TEMPP} – V_{TEMPN}$	0.177	0.178	0.179	
δ℃	Accuract of Temp.	Single point calibration	–3		3	°C
External Temperature Sensor - V_{CC} = 4.4V to 26V						
V_{IN}	Input voltage range	TS1, TS2, TS3, TS4, VBIAS = VREF1	–0.2		0.8 × V_{REF1}	V
		TS1, TS2, TS3, TS4, VBIAS = VREG	–0.2		0.8 × V_{REG}	V
$R_{NTC(PU)}$	Internal pullup resistance	TS1, TS2, TS3, TS4	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$	Resistance drift Over temperature	TS1, TS2, TS3, TS4	–360	–280	–200	PPM/°C
Internal 2.0V LDO - V_{CC} = 4.4V to 26V						
V_{REG}	LDO Regulator voltage		1.9	2	2.1	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25		%
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT}=10 mA	–0.6		0.5	%
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5		1.5	%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{REG}	Regulator output current limit	V_{REG} = 0.9 × $V_{REG(NOM)}$, V_{IN} > 4.4V	20			mA
I_{SC}	Regulator shortcircuit current limit	V_{REG} = 0 × $V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$, I_{REG} =10mA ,V_{IN} > 2.5V, f =10Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.78	1.85		V
Internal 1.5V LDO - V_{CC} = 4.4V to 26V						
V_{REG15}	LDO regulator voltage		1.35	1.5	1.65	V
V_{PORth}	POR raise threshold	Raise threshold	1.2		1.45	V
V_{PORhys}	POR hysteresis Voltage	Hysteresis Voltage		0.1		V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 40 mA		±0.25		%
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT} = 40 mA	–0.6		0.5	%
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 40 mA	–1.5		1.5	%
I_{REG}	Regulator output current limit	V_{REG} = 0.9 × $V_{REG(NOM)}$, V_{IN} > 4.4V	30			mA
Internal 3.3V LDO - V_{CC} = 4.4V to 26V						
V_{REGRTC}	3.3V regulator voltage	3.3V LDO output	3.135	3.3	3.465	V
I_{LOAD}	Regulator output current			20	30	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25		V
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT}=10 mA	–0.6		0.50	%
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5		1.50	%
R_{SW}	Switch resistance			5	6.5	Ω
I_{OCP}	Over current protection		50	100	150	mA
Low-Frequency Oscillator - V_{CC} = 4.4V to 26V						
f_{LFO}	Operating frequency			524.288		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = -20°C to 70°C, includes frequency drift	–1.5	±0.25	1.5	%
		T_A = -40°C to 85°C, includes frequency drift	–2.5	±0.25	2.5	%
$f_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz
High-Frequency Oscillator - V_{CC} = 4.4V to 26V						
F_{HFO}	Operating frequency			24		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = -20°C to 70°C, includes frequency drift	–2.5	±0.25	2.5	%
		T_A = -40°C to 85°C, includes frequency drift	–3.5	±0.25	3.5	%
$t_{HFO(SU)}$	Frequency set-up time	T_A = -20°C to 85°C, oscillator frequency within ±3% of nominal			4	mS
		oscillator frequency within ±3% of nominal			100	µS
Voltage Reference 1 - V_{CC} = 4.4V to 26V						
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = -40°C to 85°C, after trim		±80		

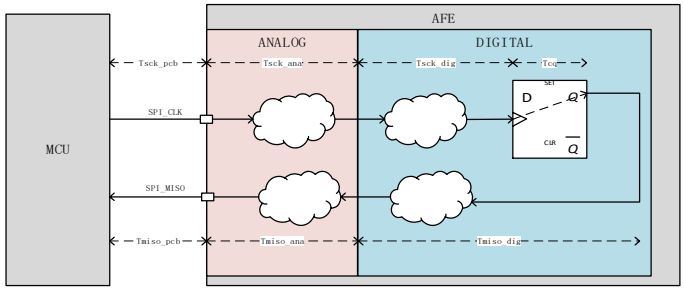
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference 2 - V_{CC} = 4.4V to 26V						
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±20		PPM/°C
		T_A = -40°C to 85°C, after trim		±30		
Instruction Flash - V_{CC} = 4.4V to 26V						
IDD_{READ}	Read current	CE=V_{IH}, all I/O's open Address input = V_{IL}/V_{IH}, and sequentially incremented at f=1/T_{RC}, V_{DD}=V_{DDMAX}		1.5	2.5	mA
IDD_{PROG}	Program current	CE=WE=V_{IH}, RE=V_{IH}, V_{DD}=V_{DDMAX}			2	mA
IDD_{ERASE}	Sector/Chip erase current	CE=WE=V_{IH}, RE=V_{IH}, V_{DD}=V_{DDMAX}			1.5	mA
Iwakeup	Wake up time current	CE=V_{IL}, DPSTB=V_{IL}, V_{DD}=V_{DDMax}, @FWUP=0			4	mA
		CE=V_{IL}, DPSTB=V_{IL}, V_{DD}=V_{DDMax}, @FWUP=1			6	mA
$I_{SB(2)}$	Standby Current	CE=V_{IL}, V_{DD}= V_{DDMAX}, all inputs are static		100		uA
$I_{DEP(2)}$	Deep Standby current	CE=V_{IL}, DPSTB=V_{IH}, V_{DD}= V_{DDMAX}, all inputs are static		0.3	15	uA
V_{IL}	Input Low Voltage	V_{DD}=V_{DDMax}			0.1xV_{DD}	V
V_{IH}	Input High Voltage	V_{DD}=V_{DDMax}	0.9xV_{DD}			V
V_{OL}	Output Low Voltage	V_{DD}= V_{DDMAX}, I_{OL} = 200uA			0.1xV_{DD}	V
V_{OH}	Output High Voltage	V_{DD}=V_{DDMIN}, I_{OH} = 150uA	0.9xV_{DD}			V
T_{DR}	Data retention	100year@25°C, 20year@105°C	20			Years
N_{END}	Sector Endurance		100,000			Cycle
OCD, SCC, SCD1, SCD2 and CD_TB Current Protection Thresholds - V_{CC} = 4.4V to 26V						
V_{OCD}	OCD detection threshold voltage range	V_{OCD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	–16.6		–100	mV
		V_{OCD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	–8.3		–50	
ΔV_{OCD}	OCD detection threshold voltage program step	V_{OCD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1		–5.56		mV
		V_{OCD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0		–2.78		
V_{SCC}	SCC detection threshold voltage range	V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	44.4		200	mV
		V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	22.2		100	
ΔV_{SCC}	SCC detection threshold voltage program step	V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1		22.2		mV
		V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0		11.1		
V_{SCD1}	SCD1 detection threshold voltage range	V_{SCD1} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		V_{SCD1} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	

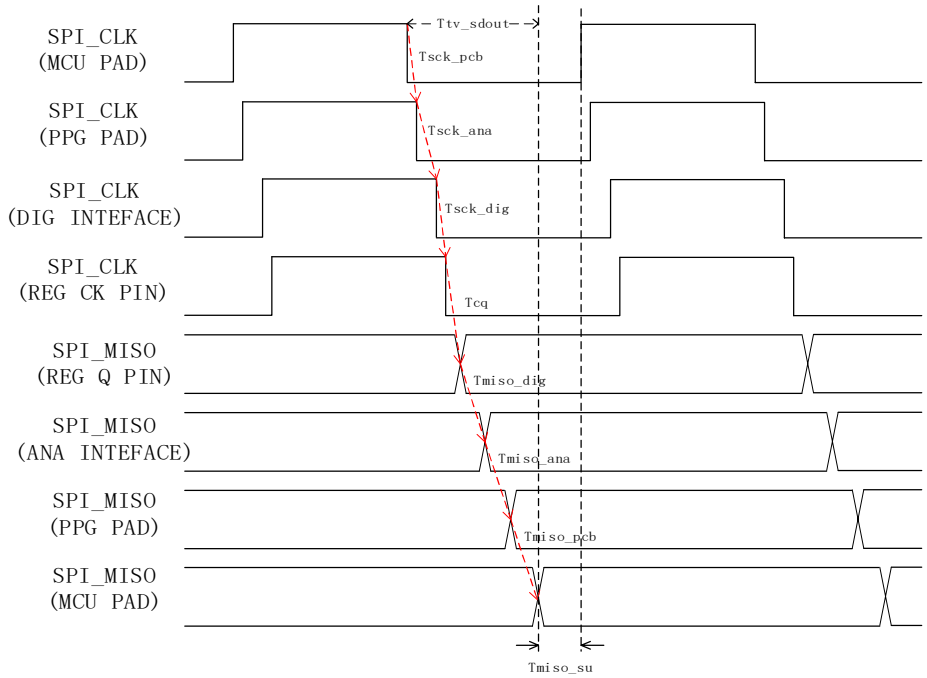
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{SCD_TB}	SCD_TB detection threshold voltage range	$V_{SCD\_TB} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–11.1		–50	mV
		$V_{SCD\_TB} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–5.5		–25	
ΔV_{SCD_TB}	SCD_TB detection threshold voltage program step	$V_{SCD\_TB} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–5.5		mV
		$V_{SCD\_TB} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–2.75		
V_{OFFSET}	OCD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OCD, SCC, and SCDx scale error	No trim	–10		10	%
		Post-trim	–5		5	
OCD, SCC, SCD1, SCD2 and CD_TB Current Protection Timing - V_{CC} = 4.4V to 26V						
t_{OCD}	OCD detection delay time		1		31	mS
Δt_{OCD}	OCD detection delay time program step			2		mS
t_{SCC}	SCC detection delay time		0		915	µS
Δt_{SCC}	SCC detection delay time program step			61		µS
t_{SCD1}	SCD1 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		915	µS
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		1850	
Δt_{SCD1}	SCD1 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		61		µS
		AFE PROTECTION CONTROL[SCDDx2] = 1		121		
t_{SCD2}	SCD2 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		458	µS
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		915	
Δt_{SCD2}	SCD2 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		30.5		µS
		AFE PROTECTION CONTROL[SCDDx2] = 1		61		
t_{CD_TB}	CD_TB detection delay time	AFE PROTECTION CONTROL[CDTBx2] = 0	0		458	µS
		AFE PROTECTION CONTROL[CDTBx2] = 1	0		915	
Δt_{CD_TB}	CD_TB detection delay time program step	AFE PROTECTION CONTROL[CDTBx2] = 0		30.5		µS
		AFE PROTECTION CONTROL[CDTBx2] = 1		61		
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OCD, SCD1, and SC2, $V_{SRP} – V_{SRN} = V_T + 3$ mV for SCC			160	µS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10		10	%
Timing Requirements: SMBus 3.1 - V_{CC} = 4.4V to 26V						
V_{IH}	Input High Voltage		1.35		V_{DD}	V
V_{HYS}	Switchover voltage hysteresis		0.08			V
V_{IL}	Input Low Voltage				0.8	V
V_{OL}	Outpput Low Voltage	I_{OL}=-20mA			0.4	V
I_{OL}	Low level output current	V_{OL}=0.4	–20			mA
$I_{LEAK-BUS}$	Leakage current		–200		200	uA
C_{BUS}	V_{BUS} capacitance				400	pF
f_{SMB}, f_{SCL}	SMBus operating frequency		10		1,000	kHz
$t_{TIMEOUT}$	Error signal detect time		25		35	mS
t_{HIGH}	Clock high period		0.26		50	uS
$t_{LOW:SEXT}$	Cumulative clock low slave extend time				25	mS
$t_{LOW:MEXT}$	Cumulative clock low master extend time				10	mS
t_F	Clock fall time				120	nS
t_{POR}	Recovery time				500	mS
Timing Requirements: UART - V_{CC} = 4.4V to 26V						
V_{DD}	Supply Powert Input		3.135	3.3	3.465	V
C_{BUS}	Load capacitance				100	pF
f_{txd}, f_{rxd}	UART operating frequency		10		1000	kHz
Timing Requirements: SPI - V_{CC} = 4.4V to 26V						
Duty	SPI_CLK duty cycle		40	50	60	%
t_{SCLK}	SPI_CLK clock perior		0.1	-	2	uS
t_{S_CS}	SPI_CS set-up time		40	-	-	nS
t_{S_SDIN}	SPI_MOSI set-up time		20	-	-	nS
t_{H_SDIN}	SPI_MOSI hold time		20	-	-	nS
t_{V_SDOUT}	SPI_MISO valuaeble time		-	-	30	nS



SPI Timing Diagram





SPI Timing Sequence Diagram

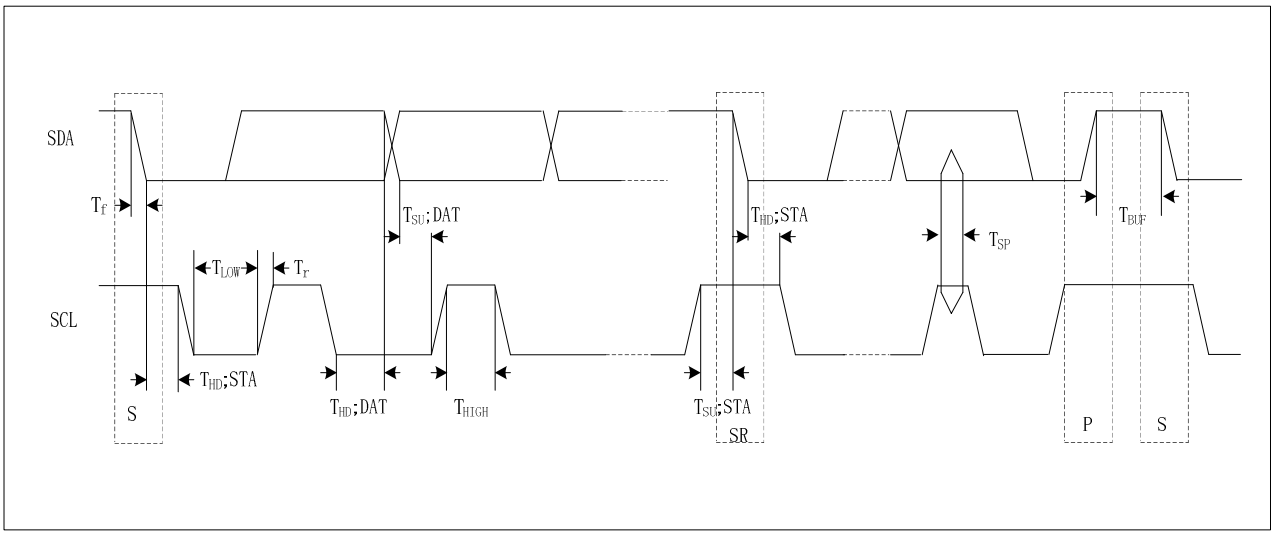
PARAMETER	MODE	TEST CONDITION	MCU TEST CONDITION	MIN	TYP	MAX	UNIT
I_{NORMAL}	Normal Mode	VADC=ON, ADC_FILTER=ON, CC=ON, CC_FILTER=ON, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=ON, VMBC=OFF	CPU=ACTIVE, HFO=ON, RTC=ON, No Communication		7.6	9.2	mA
		VADC=ON, ADC_FILTER=ON, CC=ON, CC_FILTER=ON, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=ON, VMBC=OFF	CPU=SLEEPING, HFO=ON, RTC=ON, No Communication		4.1	5	mA
		VADC=ON, ADC_FILTER=ON, CC=ON, CC_FILTER=ON, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=OFF, VMBC=ON	CPU=ACTIVE, HFO=ON, RTC=ON, No Communication		8.6	10.5	mA
		VADC=ON, ADC_FILTER=ON, CC=ON, CC_FILTER=ON, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=OFF, VMBC=ON	CPU=SLEEPING, HFO=ON, RTC=ON, No Communication		5.1	6.2	mA
I_{SLEEP}	SLEEP Mode	VADC=OFF, ADC_FILTER=OFF, CC=OFF, CC_FILTER=OFF, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=ON, VMBC=OFF	CPU=SLEEPING, HFO=OFF, RTC=ON, No Communication (5.5uA)		96.5	116	uA
		VADC=OFF, ADC_FILTER=OFF, CC=OFF, CC_FILTER=OFF, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=ON, DSG=OFF, VMBC=ON	CPU=SLEEPING, HFO=OFF, RTC=ON ,No Communication (5.5uA+0.15uA)		96.5	116	uA
		VADC=OFF, ADC_FILTER=OFF, CC=OFF, CC_FILTER=OFF, LFO=ON, LDO2V=ON, LDO5V=O N, LDO3V3=ON, LDO1P5V=ON, CHG=OFF, DSG=ON, VMBC=OFF	CPU=SLEEPING, HFO=OFF, RTC=ON, No Communication (5.5uA+0.15uA)		77	96	uA
		VADC=OFF, ADC_FILTER=OFF, CC=OFF, CC_FILTER=OFF, LFO=ON, LDO2V=ON, LDO5V=ON, LDO3V3=ON, LDO1P5V=ON, CHG=OFF, DSG=OFF, VMBC=OFF	CPU=SLEEPING, HFO=OFF, RTC=ON, No Communication (5.5uA+0.15uA)		44.5	54	uA
$I_{SHUTDOWN}$	SHUTDOWN Mode	ADC_FILTER=OFF, CC_FILTER=OFF, LFO=OFF, LDO2V=OFF, LDO5V=OFF, LDO3V3=ON, LDO1P5V=OFF, CHG=OFF, DSG=OFF, VADC=OFF, CC=OFF, SW/PA10/PA11 Pull Up ON (LDO3V3 1.3uA, NFET DRV 2.2uA)	CPU=SLEEPING, HFO=OFF, RTC=ON, No Communication (3.5uA, POR, BANDGAP, LDO1P5V, RTC)		7	10	uA
		ADC_FILTER=OFF, CC_FILTER=OFF, LFO=OFF, LDO2V=OFF, LDO5V=OFF, LDO3V3=ON, LDO1P5V=OFF, CHG=OFF, DSG=OFF, VADC=OFF, CC=OFF, SW/PA10/PA11 Pull Up ON (LDO3V3 1.3uA, NFET DRV 2.2uA)	CPU=SLEEPING, HFO=OFF, RTC=OFF, No Communication (3uA,POR, BANDGAP, LDO1P5V)		6.5	9.5	uA

Power Consumption Table

ELECTRICAL CHARACTERISTICS – I2C Communication

Symbol	PARAMETER	STD MODE		FAST MODE		ULTRA-FAST MODE		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{DD}	Operating Voltage	1.62	5.5	1.62	5.5	1.62	5.5	V
F_{SCL}	Operating frequency	0	100	0	400	0	1000	KHz
$T_{HD:START}$	Hold time of START	4	-	0.6	-	0.24	-	μS
T_{LOW}	Clock low period	4.7	-	1.3	-	0.52	-	μS
T_{HIGH}	Clock high period	4	-	0.6	-	0.24		μS
$T_{SU:START}$	Set-up time of START signal	4.7	-	0.6	-	0.24		μS
$T_{HD:DATA}$	Hold time	0	3.45	0	0.9	0	0.36	μS
$T_{SU:DATA}$	Set-up time	250	-	100	-	50		nS
T_R	Rise time of SCL and SDA	-	1000	20+0.1Cb(1)	300	-	120	nS
T_F	Fall time of SCL and SDA	-	300	20+0.1Cb(1)	300	-	120	nS
$T_{SU:STOP}$	Set-up time of STOP	4	-	0.6	-	-	0.24	μS
T_{BUF}	Bus free time between start and stop	4.7	-	1.3	-	0.52	-	μS
T_{SP}		N/A	N/A	0	50	0	20	nS

(1) Cb means the capacitance of whole line. The unit is pF.

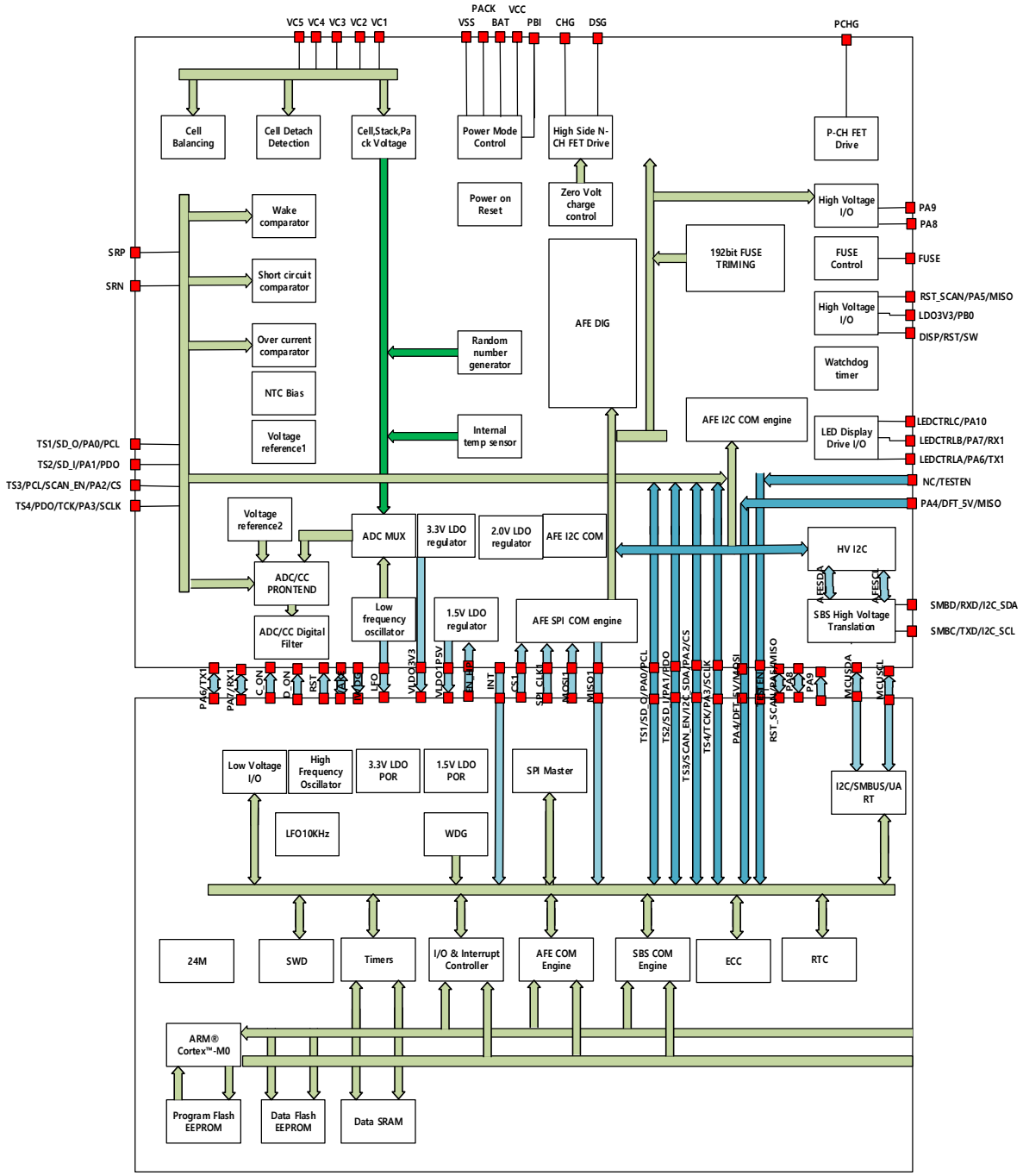


I2C Standard and Fast-Mode Timing Diagram

FEATURE DESCRIPTION

PJ67250 is a battery pack-based single-chip fully integrated solution that provides a series of feature-rich single-chip solutions for power monitoring, protection and certification of 2-series, 3-series, and 4-series cell lithium-ion and lithium-polymer battery packs. PJ67250 has battery life monitoring, high-precision remaining power detection and lithium battery protection functions.

FUNCTIONAL BLOCK DIAGRAM



Primary (1st Level) Safety Features

PJ67250 is configured to provide more extensive protection for batteries and battery systems. The following is a detailed explanation of the status flag bits of level one protection.

NAME	Primary (1st Level) Safety Features	
CUV	Cell Undervoltage Protection	0 - Normal
		1 - Happened
CUVC	Cell Undervoltage Protection Compensated	0 - Normal
		1 - Happened
COV	Cell Overvoltage Protection	0 - Normal
		1 - Happened
OCC	Overcurrent in Charge Protection	0 - Normal
		1 - Happened
		0 - Normal
OCD	Overcurrent in Discharge Protection	1 - Happened
		0 - Normal
		1 - Happened
AOLD	Overload in Discharge Protection	0 - Normal
		1 - Happened
ASCC	Short Circuit in Charge Protection	0 - Normal
		1 - Happened
ASCD	Short Circuit in Discharge Protection	0 - Normal
		1 - Happened
OTC	Overtemperature in Charge Protection	0 - Normal
		1 - Happened
OTD	Overtemperature in Discharge Protection	0 - Normal
		1 - Happened
OTF	Overtemperature CHG/DSG FET protection	0 - Normal
		1 - Happened
UTC	Undertemperature in Charge Protection	0 - Normal
		1 - Happened
UTD	Undertemperature in Discharge Protection	0 - Normal
		1 - Happened
SBSWF	Host Watchdog Timeout Protection	0 - Normal
		1 - Happened
PTO	Precharge Timeout Protection	0 - Normal
		1 - Happened
CTO	Fast Charge Timeout Protection	0 - Normal
		1 - Happened
OC	Overcharge Protection	0 - Normal
		1 - Happened
CHGV	Overcharging Voltage Protection	0 - Normal
		1 - Happened
CHGC	Overcharging Current Protection	0 - Normal
		1 - Happened
PCHGC	Over Precharge Current Protection	0 - Normal
		1 - Happened

Secondary (2nd Level) Safety Features

The secondary safety features of the PJ67250 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging.

NAME	Secondary (2nd Level) Safety Features	
SUV	Safety Undervoltage Permanent Failure	0 - Normal
		1 - Happened
SOV	Safety Overvoltage Permanent Failure	0 - Normal
		1 - Happened
SOCC	Safety Overcurrent in Charge Permanent Failure	0 - Normal
		1 - Happened
SOCD	Safety Overcurrent in Discharge Permanent Failure	0 - Normal
		1 - Happened
SOT	Safety Overtemperature Permanent Failure	0 - Normal
		1 - Happened
SOTF	Safety FET Overtemperature Permanent Failure	0 - Normal
		1 - Happened
QIM	Qmax Imbalance Permanent Failure	0 - Normal
		1 - Happened
CB	Cell Balancing Permanent Failure	0 - Normal
		1 - Happened
IMP	Impedance Imbalance Permanent Failure	0 - Normal
		1 - Happened
CD	Capacity Degradation Permanent Failure	0 - Normal
		1 - Happened
VIMR	Voltage Imbalance at Rest Permanent Failure	0 - Normal
		1 - Happened
VIMA	Voltage Imbalance Active Permanent Failure	0 - Normal
		1 - Happened
CFET	Charge FET Permanent Failure	0 - Normal
		1 - Happened
DFET	Discharge FET Permanent Failure	0 - Normal
		1 - Happened
FUSE	Fuse Failure Permanent Failure	0 - Normal
		1 - Happened
AFERF	AFE Register Permanent Failure	0 - Normal
		1 - Happened
AFEC	AFE Communication Permanent Failure	0 - Normal
		1 - Happened
2LVL	Second Level Protector Permanent Failure	0 - Normal
		1 - Happened
IFCF	Instruction Flash Checksum Permanent Failure	0 - Normal
		1 - Happened
DFW	Data Flash Permanent Failure	0 - Normal
		1 - Happened
OTF	Open Thermistor Permanent Failure	0 - Normal
		1 - Happened

Operating Status Report

PJ67250 can feedback the current operating status through SMBus and promptly feedback the current status of the battery management system to the system.

Operating Status	
Name	**Description**
PRES	Whether the battery is connected to the application system
	0 – No
	1 – Yes
FAS	Whether it is in Full Access mode
	0 – No
	1 – Yes
SS	Whether it is in Sealed mode
	0 – No
	1 – Yes
CSV	Whether Check Sum has been generated
	0 – No
	1 – Yes
WAKE	Whether it is in the Wake-Up stage
	0 – No
	1 – Yes
DSG	Whether it is in Discharge state
	0 – No
	1 – Yes
XDSG	Whether it is in a Discharge-Prohibited state
	0 – No
	1 – Yes
DUE	Data update error flag
	0 – No
	1 – Yes
XCHG	Is the battery in Charging-Prohibited state
	0 – No
	1 – Yes
CHGSUSP	Is the battery in a Charging-Suspended state?
	0 – No
	1 – Yes
PCHG	Is the battery in a Pre-Charged state?
	0 – No
	1 – Yes
MCHG	Is the battery in Trickle-Charge state?
	0 – No
	1 – Yes
LTCHG	Is the battery in a Low Temperature Charging state?
	0 – No
	1 – Yes

Name	Description
ST1CHG	Is the battery charging at Standard Temperature state 1?
	0 – No
	1 – Yes
ST2CHG	Is the battery charging at Standard Temperature state 2?
	0 – No
	1 – Yes
HTCHG	Is the battery in a High Temperature Charging state?
	0 – No
	1 – Yes
CB	Is the battery in a Cell Balance state?
	0 – No
	1 – Yes
OC	Is the battery voltage in an Overcharged state?
	0 – No
	1 – Yes

Charge Control Features

The PJ67250 charge control features include :

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two subranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

Gas Gauging

PJ67250 accurately measures the remaining battery capacity based on the impedance measurement algorithm. The remaining capacity is measured by integrating the charging current and the discharging current, and the charging current is compensated in real time by the SOC status and temperature of the battery. PJ67250 will estimate the battery's pre-discharge and adjust the estimated value of the battery's self-discharge based on the

current temperature. PJ67250 supports TURBO 3.0 mode. TURBO 3.0 can tell the MCU the peak power and peak voltage of the battery that will not cause the system to reset and stop working.

Configuration

PJ67250 accurately measures the remaining battery capacity based on the impedance measurement algorithm.

- **Oscillator Function**

  The PJ67250 integrated the system clock by internal RC and does not require any external components.

- **2-Series, 3-Series, or 4-Series Cell Configuration**

  When PJ67250 is configured for a 2-cell battery application, VC4, VC3, and VC2 are short-circuited. When configured for 3-cell applications, VC4 and VC3 are shorted.

- **Cell Balancing**

  PJ67250 supports battery balancing through bypass charging current during charging. The internal balancing bypass current can be up to 20mA. If a larger current needs to be bypassed, it can be achieved through external balancing.

Battery Parameter Measurements

- **Charge and Discharge Counting**

  PJ67250 integrates two ADCs, one SDADC for current measurement, and a second-order SDADC for battery voltage and temperature measurement.

  One SDADC measures the charge and discharge current by measuring the current sensing resistor between SRP and SRN. The measurement range of this SDADC is -0.1V~0.1V. When $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, it means the system is charging the battery. When $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative, it means the system is discharging the battery.

Battery Trip Point (BTP)

The battery trip point (BTP) represents battery life, and this value is stored in the DF register. BTP can be set by the host with two capacity threshold points to ensure that an interrupt is generated when BTP is triggered, and the interrupt is output from BTP_INT. When BTP is triggered, BTP has a weak pull-up inside the chip.

Battery Lifetime Data Logging Features

The PJ67250 has several key battery parameters to record battery life. The following parameters will be updated every 10 hours if there is a difference between RAM and Data Flash.

Name	Number	Descriptions
MAXCV	1	Maximum Cell Voltages
MINCV	2	Minimum Cell Voltages
MAXDCV	3	Maximum Delta Cell Voltage
MAXCC	4	Maximum Charge Current

Name	Number	Descriptions
MAXDC	5	Maximum Discharge Current
MAXADC	6	Maximum Average Discharge Current
MAXADP	7	Maximum Average Discharge Power
MAXCT	8	Maximum Cell Temperature
MINCT	9	Minimum Cell Temperature
MAXDCT	10	Maximum Delta Cell Temperature
MAXIST	11	Maximum Internal Sensor Temperature
MINIST	12	Minimum Internal Sensor Temperature
MAXFETT	13	Maximum FET Temperature
NSEOCOO	14	Number of Safety Events Occurrences and the Last Cycle of the Occurrence
NCTALC	15	Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
NQRUAC	16	Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
NOSD	17	Number of Shutdown Events
CBTC	18	Cell Balancing Time for Each Cell (This data is updated every 2 hours if a difference is detected.)
TRTASET	19	Total FW Runtime and Time Spent in Each Temperature Range (This data is updated every 2 hours if a difference is detected.)

Authentication

The PJ67250 supports authentication by the host using SHA-1/ SHA-256.

The PJ67250 supports ECC authentication.

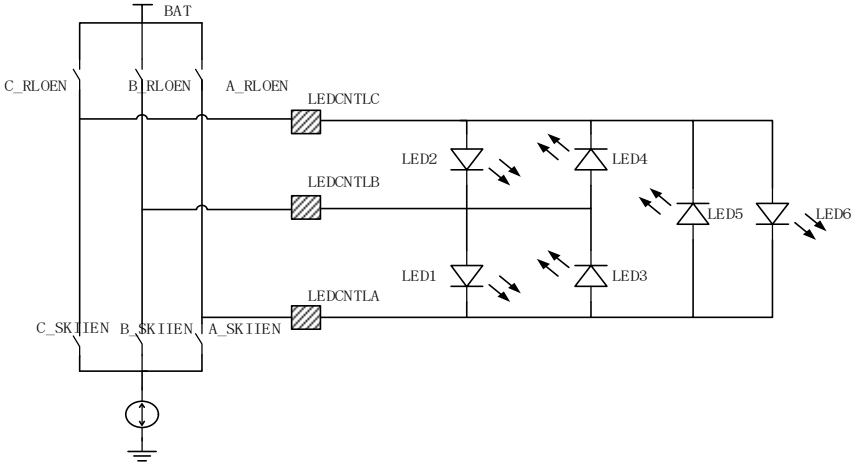
LED Power Display

PJ67250 supports 3-, 4-, 5-, and 6-segment LED power display, and supports battery failure LED display. The LED display supports automatic scanning and manual scanning.

Manual scanning supports 3-, 4-, 5-, 6-segment LED power display. Automatic scanning supports 4-, 5-, and 6-segment LED power display. The LED display brightness supports adjustable Duty levels of 1~256.

Clock	LED-Segment	LEDCKS[1:0]	Pre-Segment	Actual Frequency (Hz)
131kHz	6	00	1	85.29
	6	01	2	42.64
	6	1x	4	21.32
	5	00	1	102.34
	5	01	2	51.17
	5	1x	4	25.59
	4	00	1	127.93
	4	01	2	63.96
	4	1x	4	31.98

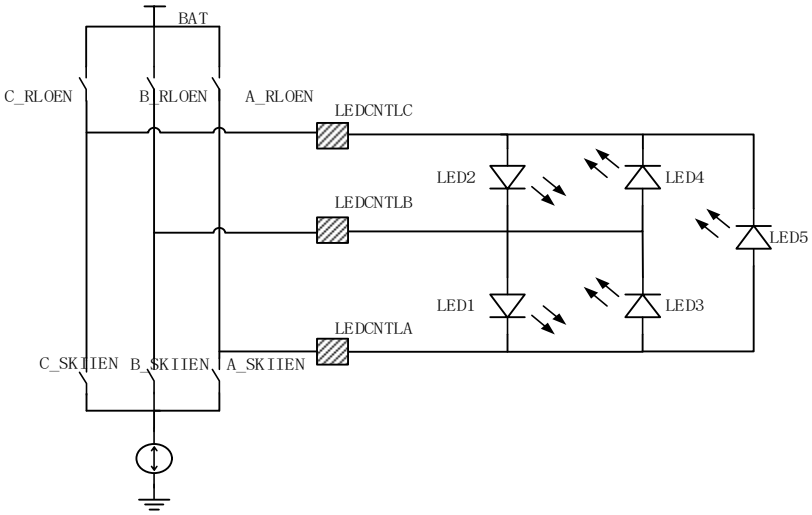
■ Drive for 6 LEDs



LED Number configuration is 6								
LEDCNTLA	**LEDCNTLB**	**LEDCNTLC**	**LED1**	**LED2**	**LED3**	**LED4**	**LED5**	**LED6**
Pull-Up	Pull-Down	Floating	Off	Off	On	Off	Off	Off
Pull-Up	Floating	Pull-Down	Off	Off	Off	Off	On	Off
Pull-Down	Pull-Up	Floating	On	Off	Off	Off	Off	Off
Floating	Pull-Up	Pull-Down	Off	Off	Off	On	Off	Off
Pull-Down	Floating	Pull-Up	Off	Off	Off	Off	Off	On
Folating	Pull-Down	Pull-Up	Off	On	Off	Off	Off	Off

6 LEDs Display Table

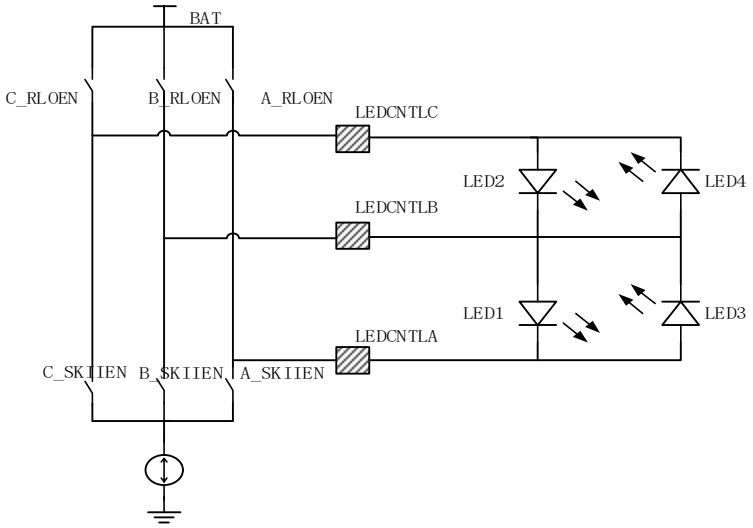
■ Drive for 5 LEDs



LED Number configuration is 5							
LEDCNTLA	**LEDCNTLB**	**LEDCNTLC**	**LED1**	**LED2**	**LED3**	**LED4**	**LED5**
Pull-Up	Pull-Down	Floating	Off	Off	On	Off	Off
Pull-Up	Floating	Pull-Down	Off	Off	Off	Off	On
Pull-Down	Pull-Up	Floating	On	Off	Off	Off	Off
Floating	Pull-Up	Pull-Down	Off	Off	Off	On	Off
Pull-Down	Floating	Pull-Up	-				
Folating	Pull-Down	Pull-Up	Off	On	Off	Off	Off

5 LEDs Display Table

■ **Drive for 4 LEDs**



LED Number configuration is 4						
LEDCNTLA	**LEDCNTLB**	**LEDCNTLC**	**LED1**	**LED2**	**LED3**	**LED4**
Pull-Up	Pull-Down	Floating	Off	Off	On	Off
Pull-Up	Floating	Pull-Down	-			
Pull-Down	Pull-Up	Floating	On	Off	Off	Off
Floating	Pull-Up	Pull-Down	Off	Off	Off	On
Pull-Down	Floating	Pull-Up	-			
Folating	Pull-Down	Pull-Up	Off	On	Off	Off

4 LEDs Display Table

Function description of AFE timer A

The setting range is 125ms to 64s, it can directly turn on CC for current measurement through the timer, and directly turn on VADC for polling. It can also wake up the MCU through the timer, and turn on CC and VADC through the MCU startup program.

Battery Voltage Measurement

VADC supports 21 channel measurement and up to 11 channel polling. Customers can configure 1 to 11 channel polling. It also supports single channel measurement and supports multiple averaging of single channel. During VADC measurement, it supports any conversion time from 1mS to 32mS.

Channel No.	Function Description	PGA	Measuement Range
1	AGND (Internal Short)	PGA=1/2	0V~2.4V
		PGA=1	0V~1.2V
2	VTEMPP-VTEMPN (Internal temperature sensor)	PGA=1/2	0V~2.4V
		PGA=1	0V~1.2V
3	VIN_VADC	PGA=1/2	0V~2.4V
		PGA=1	0V~1.2V
4	TS*	PGA=1/2	0V~2.4V
		PGA=1	0V~1.2V
5	VC4_DIV (BAT Voltage)	PGA=1/2	0V~2.4V x20
		PGA=1	0V~1.2V x20
6	PACK_DIV (PACK Voltage)	PGA=1/2	0V~2.4V x20
		PGA=1	0V~1.2V x20
7	VBUS_DIV (VBUS Voltage)	PGA=1/2	0V~2.4V x20
		PGA=1	0V~1.2V x20
8	PACKST (PACK Short Detection)	PGA=1/2	0V~2.4V
		PGA=1	0V~1.2V
9	VC1-0	PGA=1/5	0V~6V
10	VC2-VC1	PGA=1/5	0V~6V
11	VC3-VC2	PGA=1/5	0V~6V
12	VC4-VC3	PGA=1/5	0V~6V
13	VCC-PACK (DSG MOS Impedance Detection)	PGA=1/2	-1V~1V
14	VBAT-VCC (CHG MOS Impedance Detection)	PGA=1/2	-1V~1V
15	VCC-VBUS (VBMC MOS Impedance Detection)	PGA=1/2	-1V~1V
16	VATP-VATN (ADC Auto-Measurement)	PGA=1/2	Generated internally

Battery Currengt Measurement

PJ67250 uses the sampling resistor between SRP and SRN to measure the charge and discharge current. The sampling resistor is usually between 1mΩ and 3mΩ. It can also support 0.5mΩ resistance sampling. When setting the 0.5mΩ resistor sampling, the CC accuracy loses 1 effective bit.

Hardware protection

PJ67250 hardware protection includes OCD (Overcurrent in Discharge Protection), SCC (Short Circuit in Charge Protection), SCD1 (Short Circuit in Discharge Protection 1), SCD2 (Short Circuit in Discharge Protection 2). OCD, SCC, SCD1, and SCD2 all have separate enable controls to turn them on and off. When OCD, SCC, SCD1, and SCD2 are enabled, when any event occurs in OCD, SCC, SCD1, or SCD2, DSG/CHG and V_{BMC} will output low (V_{GS} is 0) and disconnect the MOS.

When C_ON/D_ON is set to 1, the DSG/CHG output is high (V_{GS}=11.5V around), off the MOS connection is closed.

When FLYMODE<1:0> is set to 11, the DSG/CHG output is high (V_{GS}=11.5V around) and the MOS connection is closed.

Timer

PJ67250 includes 1 advanced timer and 2 general timers

- **Advanced Timer (TIM1)**

  TIM1 is a 16-bit counter with 16-bit prescaler that can count up, down and up-down. It has four channels, all supporting input capture and output comparison. The output PWM signal can be used to control the motor or applied in power consumption management. The complementary outputs of each channel share the same embedded dead time configuration.

  TIM1 can work together with other timers through the connection feature between timers. When DMA is enabled, DMA can read and write the TIM1 register. In debug mode, you can stop the counter from counting.

- **General Timers (TIM3 and TIM14)**

  2 general-purpose timers can be used as simple time bases or output PWM.

  TIM3 is a 16-bit counter with 16-bit prescaler that can count up, down and up-down. They have four channels and all support independent input capture, output comparison and PWM generation. TIM3 can work together with other timers through the connection feature between timers. When DMA is enabled, DMA can read and write the TIM3 register. In debug mode, you can stop the counter from counting.

  TIM14 is a 16-bit counter with 16-bit prescaler and only 1 channel for input capture, output comparison and PWM generation. In debug mode, you can stop the counter from counting.

- **Low Power Consumption Timer (LPTIM1)**

  A 16-bit counting timer that can be timed in deep sleep mode 2, 3-bit prescaler, supports 1 to 128 divider. The clock source can choose internal system clock, LSE, LRC, and supports pulse output and PWM output.

- **Tick Timer (SysTick)**

  The tick timer can be used in real-time operating systems and is also a standard down counter. It is a 24-bit down counter with HCLK or HCLK/8 as the clock source and automatic reloading function. When the counter reaches 0, the tick timer generates a maskable system interrupt.

Authentication

- **Asymmetric Algorithm**
  - Support SECP 192/224/256/384/512/521, SM2
  - Support encryption/decryption
  - ECC: supports NIST SECP curve; signature, signature verification, encryption, decryption, secret key generation, point verification
  - SM2: supports signature, signature verification, encryption, decryption, secret key generation, and key exchange
- **Hash Algorithm**
  - Support SHA224/SHA256/SM3
  - Mode supports HMAC
  - Data endianness: byte swapping
- **Random Number**
  - Supports generating true/pseudo random numbers

Serial Debug Port (SWD-DP)

ARM Cortex-M0 integrates debugging components internally, and the SW debugging port is used to connect these debugging components.

The SWD function can be disabled through option configuration. The software writes this configuration to disable the SWD function; the SWD function can be unlocked by erasing this option configuration, but the hardware will erase the entire APROM and LDROM when unlocking. If the LDROM is locked, the hardware automatically unlocks the LDROM. , and erase it.

The SWD function can be permanently disabled through the chip Flash read and write protection mechanism and cannot be restored.

LDROM

The chip has a built-in 16KB/32KB/64KB LDROM with configurable size. The LDROM is customer programmable and supports locking through option configuration. After locking, erasing and writing operations cannot be performed to protect the LDROM from being accidentally rewritten. By unlocking the SWD function, the hardware will erase the entire APROM and LDROM. If the LDROM is locked, the hardware will automatically unlock the LDROM and erase it. This method is the only way to unlock the LDROM.

Out of order Powered on of VC1 to VC4, and BAT

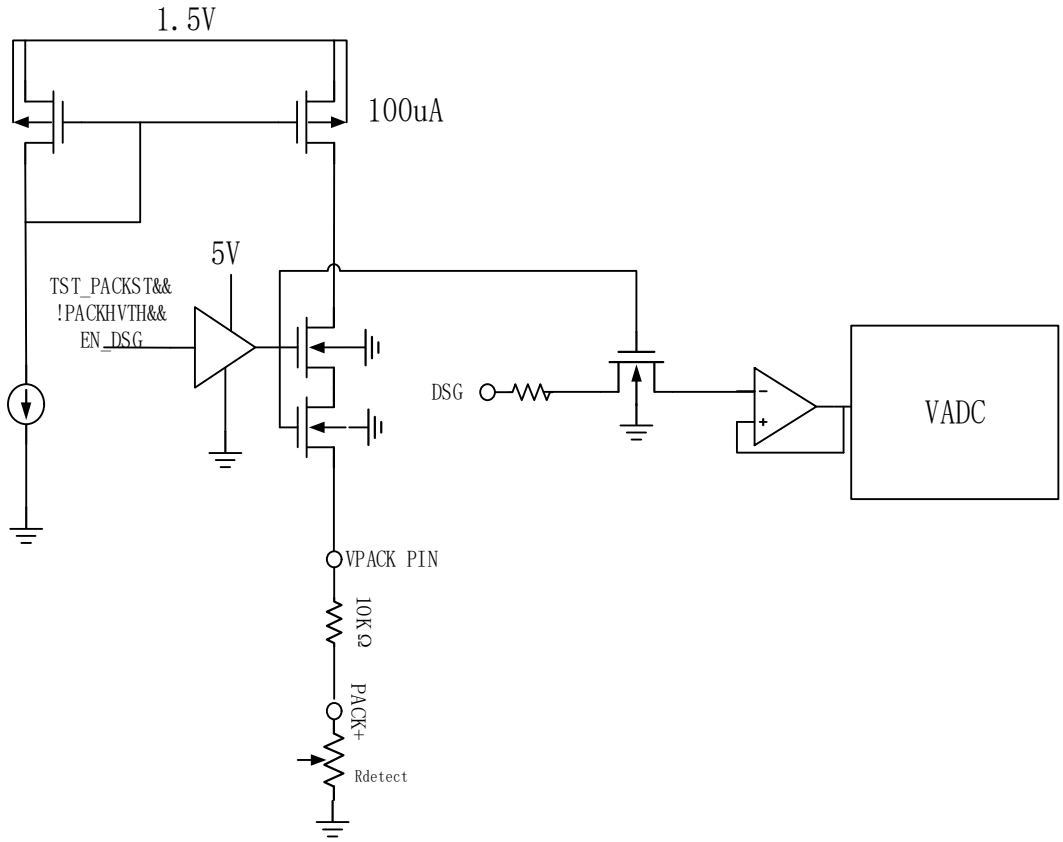
PJ67250 supports out-of-order power-on of BAT and VC1 to VC4. Powering on high-voltage pins first will not cause overvoltage damage to low-voltage pins; voltage jitter during power-on will not cause accidental erasure or damage to the Flash in the chip.

Golden Key

PJ67250 built-in 4KB area for Golden key and only supports one time write. After writing, the hardware automatically performs verification and cannot be erased. The user software cannot read the data of Golden key area. Only the encryption module can read the Golden key through hardware and perform encryption/decryption related operations.

Support PACK+/PACK- short circuit protection detection

PJ67250 supports impedance detection of the battery output interface (between PACK+ and PACK-) when DSG MOS is turned off. When using this function, the MCU sends a command to start the detection signal source (TSTPACKST=1, the configuration is invalid when DSG MOS is on or PACK is inserted), and the 100uA current detection signal is excited (100uA accuracy is +/-20% accuracy) through VPACK The pin is output to the battery PACK+, and the MCU detects the battery PACK+ voltage through the VADC channel connected to the DSG pin (the detection accuracy is VPACK+/-0.2mV). The MCU detects the voltage result to determine whether the battery interface impedance is a short circuit.



C_ON/D_ON controls MOS shutdown directly

The MCU output signal can directly control the CHG/DSG MOS forced shutdown through the C_ON/D_ON pin. Even if the AFE chip is reset, the C_ON/D_ON pin directly controls the CHG/DSG MOS forced shutdown and is still valid. C_ON/D_ON controls CHG/DSG. MOS forced shutdown has the highest priority.

SMBus status detection

PJ67250 detects that SMBC and SMBD remain low for more than 2S, then it considers SMBus to be idle. To clear this state, you need to set SMBC or SMBD to high.

Power Consumption Mode

PJ67250 supports 3 power consumption modes:

- **Normal working mode:**

  PJ67250 high-precision measurement, calibration, high-precision lithium battery protection and data update every 0.25S. In other time periods, modules that are not necessary to be turned on are turned off.

- **SLEEP mode**

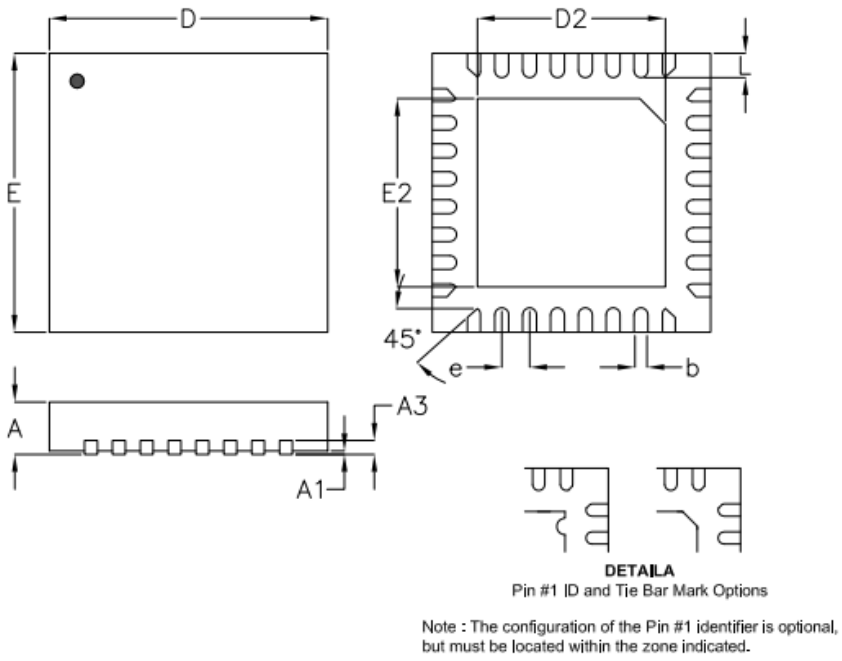
  PJ67250 high-precision measurement, calibration, high-precision lithium battery protection, the time interval for updating data is configurable, and modules that are not necessary to be turned off during other time periods are closed.

- **Shutdown mode:**

  PJ67250 is completely shut down.

PACKAGE DIMENSION

WQFN32 (4x4)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.700	2.900	0.106	0.114
E	3.900	4.100	0.154	0.161
E2	2.700	2.900	0.106	0.114
e	0.400		0.016	
L	0.250	0.350	0.009	0.013

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