

PJQ5863A-AU

60V Dual P-Channel Enhancement Mode MOSFET

Voltage	-60 V	Current	-13.6 A
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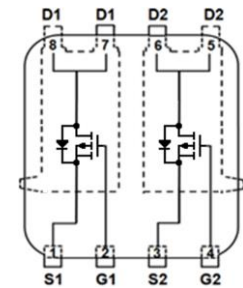
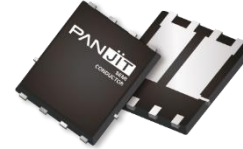
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-7.5A < 68m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-4A < 85m\Omega$
- Low Gate Charge
- High switching speed
- Improved dv/dt capability
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060B-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.092 grams

DFN5060B-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	$T_C=25^\circ\text{C}$	I_D	-13.6	A
	$T_C=100^\circ\text{C}$		-8.6	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	-55	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	23	W
	$T_C=100^\circ\text{C}$		9	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	-3.7	A
	$T_A=70^\circ\text{C}$		-3.0	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.7	W
	$T_A=70^\circ\text{C}$		1.1	
Single Pulse Avalanche Energy ^(Note 6)		E_{AS}	30	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	$R_{\theta JC}$	5.5	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	73.5	



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.6	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-7.5A	-	57	68	mΩ
		V _{GS} =-4.5V, I _D =-4A	-	75	85	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 7)						
Total Gate Charge	Q _g	V _{DS} =-30V, I _D =-7.5A, V _{GS} =-10V ^(Note 2,3)	-	17	-	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	
Gate-Drain Charge	Q _{gd}		-	3.6	-	
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHZ	-	879	-	pF
Output Capacitance	C _{oss}		-	70	-	
Reverse Transfer Capacitance	C _{rss}		-	47	-	
Turn-On Delay Time	t _{d(on)}	V _{DS} =-30V, I _D =-1A, V _{GS} =-10V, R _G =6Ω ^(Note 2,3)	-	8.4	-	ns
Turn-On Rise Time	t _r		-	30	-	
Turn-Off Delay Time	t _{d(off)}		-	52	-	
Turn-Off Fall Time	t _f		-	16	-	
Drain-Source Diode						
Diode Forward Current	I _s	T _C =25°C	-	-	-13.6	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V	-	-0.73	-1	V

NOTES :

- Pulse width ≤ 300us, Duty cycle ≤ 2%.
- Essentially independent of operating temperature typical characteristics.
- Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J = 25°C.
- The maximum current rating is package limited.
- R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- The test condition is L=0.1mH, I_{AS}= -25A, V_{DD}= -25V, V_{GS}= -10V, Starting T_J=25°C.
Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

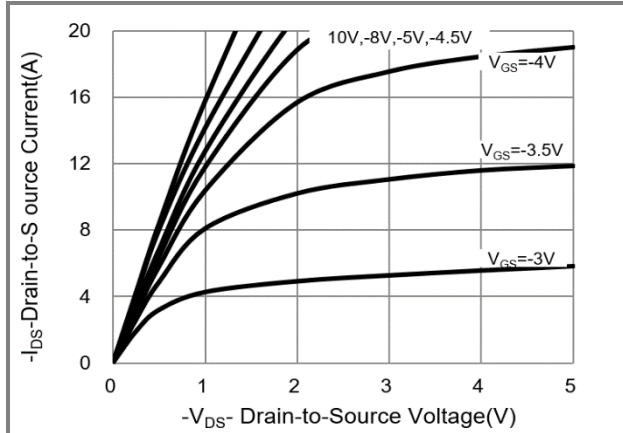


Fig.1 On-Region Characteristics

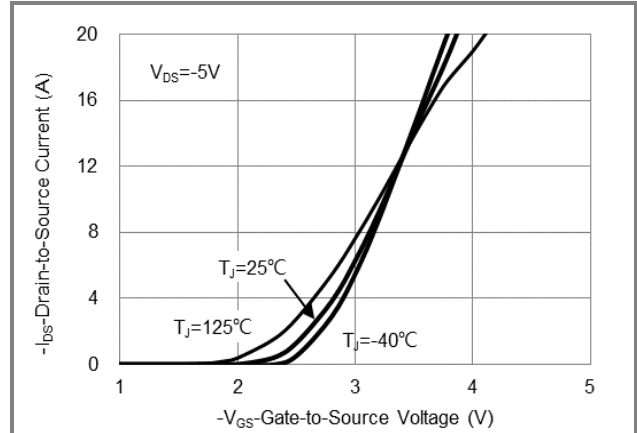


Fig.2 Transfer Characteristics

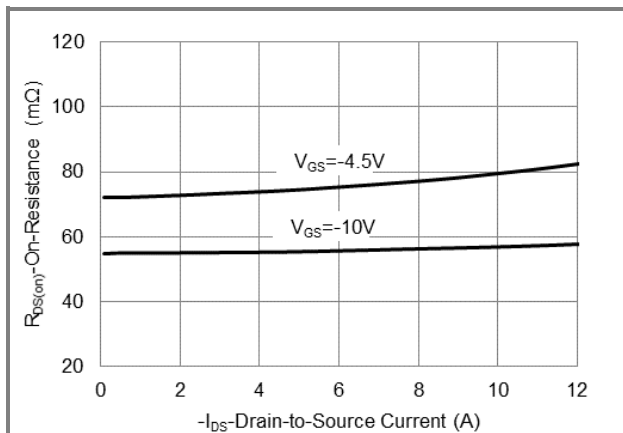


Fig.3 On-Resistance vs. Drain Current

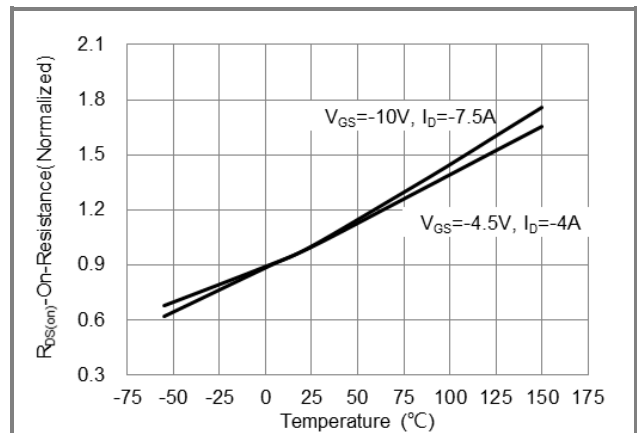


Fig.4 On-Resistance vs. Junction temperature

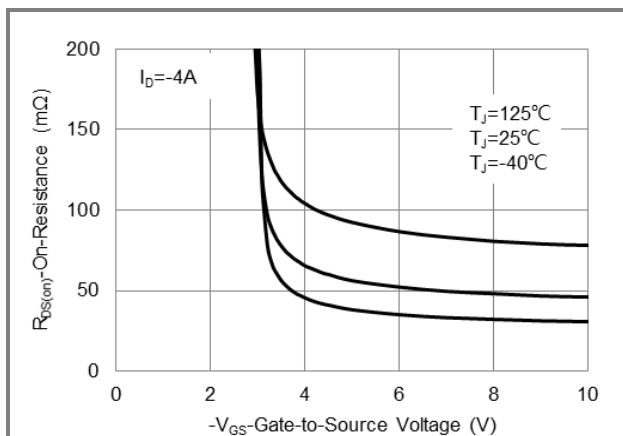


Fig.5 On-Resistance Variation with V_{GS}

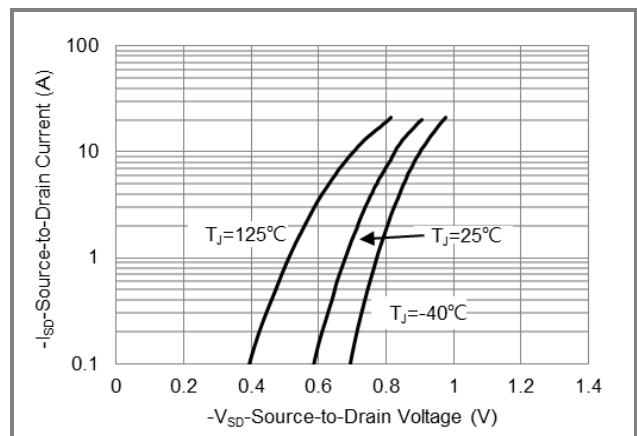


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

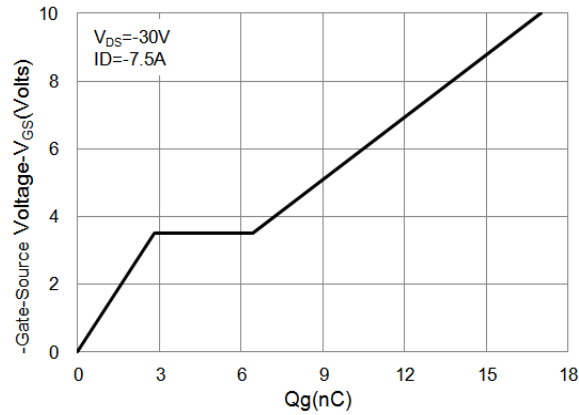


Fig.7 Gate-Charge Characteristics

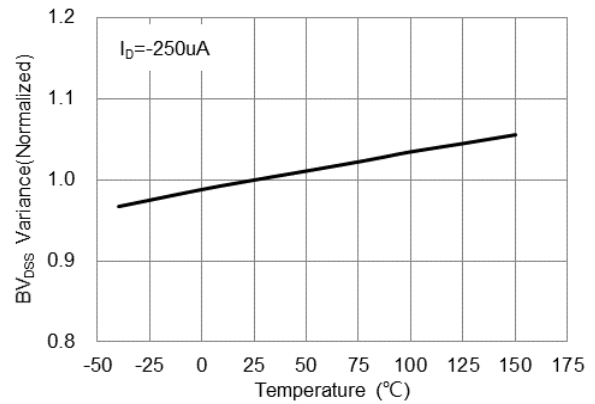


Fig.8 Breakdown Voltage Variation vs. Temperature

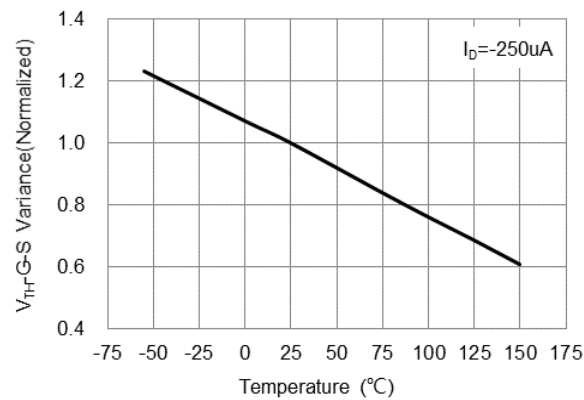


Fig.9 Threshold Voltage Variation with Temperature

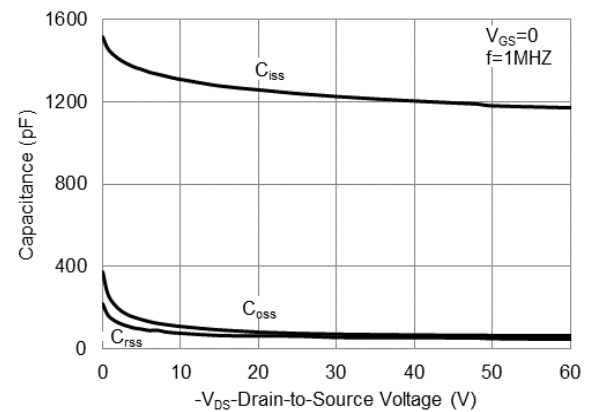


Fig.10 Capacitance vs. Drain-Source Voltage

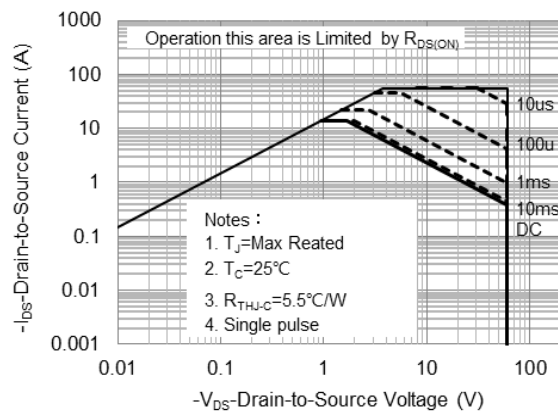


Fig.11 Maximum Safe Operating Area

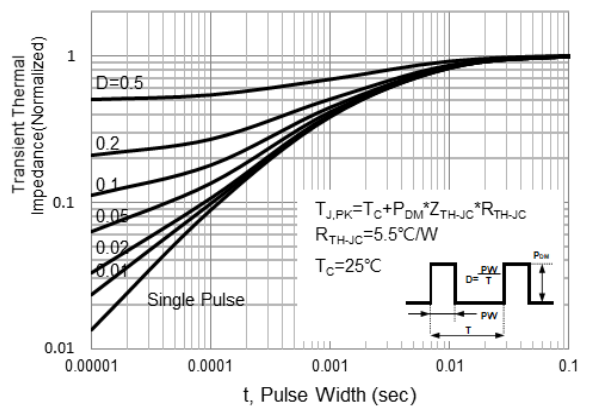


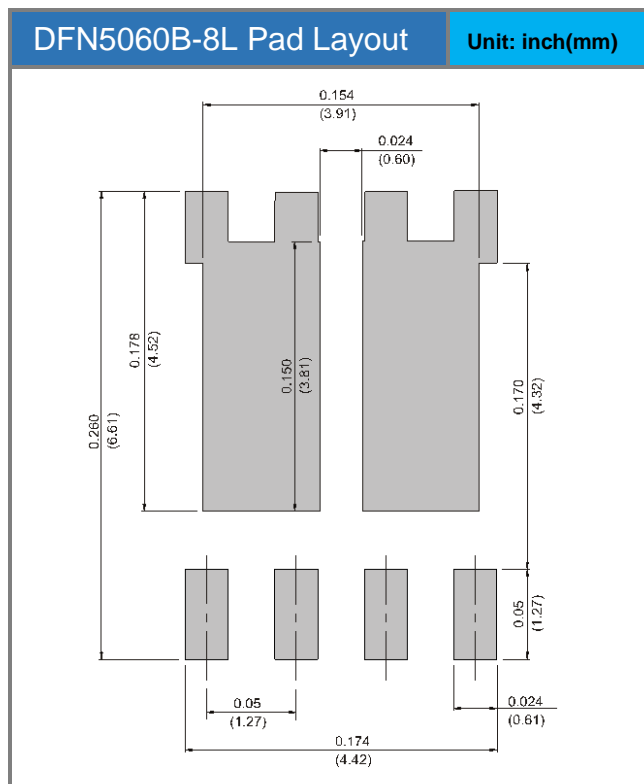
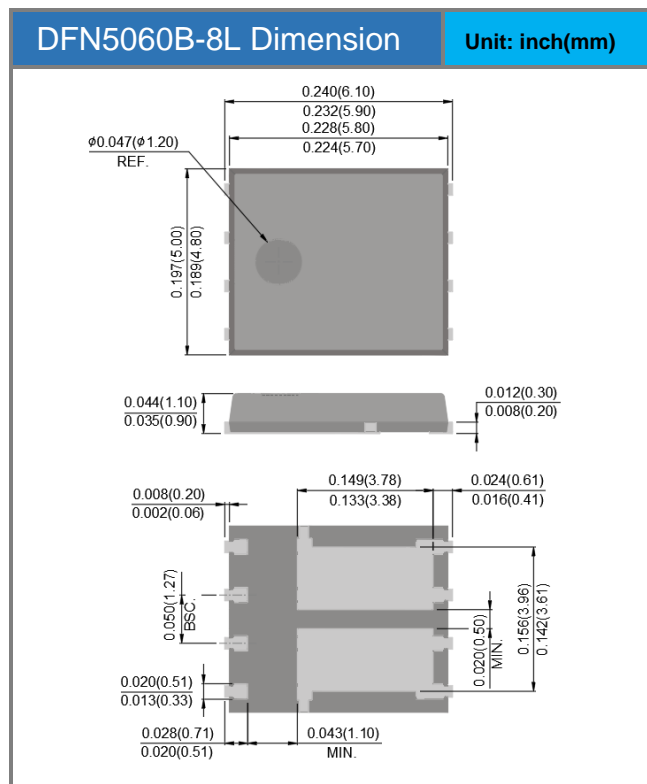
Fig.12 Normalized Transient Thermal Impedance

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Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ5863A-AU_R2_002A1	DFN5060B-8L	3K pcs / 13" reel	Q5863A	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





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