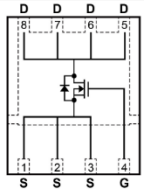
40V N-Channel Power MOSFET

BV_{DSS}	40V	$R_{DS(ON)_MAX}$	0.61mΩ
I_{D_MAX}	542A	Q_{g_TYP}	140nC

DFN5060SW-8L





Top side view

Feature

- Maximum $R_{DS(ON)}$ < 0.61mΩ at V_{GS} = 10V
- Maximum $R_{DS(ON)}$ < 0.76mΩ at V_{GS} = 7V
- N channel MOSFET - Standard Level
- Excellent FoM ($R_{DS(on)}$ x Qg)
- 175°C operating temperature
- 100% Avalanche & Rg tested
- Package with Side Wettable Flanks (SWF) for automated optical solder inspection (AOI)
- AEC-Q101 qualified and PPAP capable
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : Advanced DFN5060SW-8L Package (Patented)
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.1056 gram

Application

- DC-DC Converters
- Motor Drivers
- Automotive Applications

Absolute Maximum Ratings (T_J=25°C unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(1)	T_C=25°C	I_D	542	A
	T_C=75°C		443	
	T_C=100°C		383	
Pulsed Drain Current	T_C=25°C, t_P≤100us	I_{DM}	2863	
Power Dissipation	T_C=25°C	P_D	341	W
	T_C=75°C		227	
	T_C=100°C		170	

PARAMETER		SYMBOL	VALUE	UNIT
Continuous Drain Current (1)	T_A=25°C	I_D	65.7	A
	T_A=75°C		53.6	
	T_A=100°C		46.4	
Power Dissipation	T_A=25°C	P_D	5	W
	T_A=75°C		3.3	
	T_A=100°C		2.5	
Body Diode Continuous Current(1)	T_C=25°C	I_S	324	A
Body Diode Pulse Current	T_C=25°C, t_P≤100us	I_{SM}	2863	
Single Pulse Avalanche Current(2)		I_{AS}	80	
Single Pulse Avalanche Energy	I_{AS}=40A, limited by T_{J_MAX}	E_{AS}	2377	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	°C

Thermal Characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Thermal Resistance	Junction to Ambient(3)	$R_{\theta JA}$	–	30	–	°C/W
	Junction to Case	$R_{\theta JC}$	–	0.34	0.44	
	Junction to Case(TOP)	$R_{\theta JC_top}$	–	–	13	

Notes :

(1). The maximum continuous current of chip capability is calculated by maximum junction temperature and thermal resistance, and it will vary depending on the application and environment.

(2). L=0.1mH, 100% test in production.

(3). Surface mounted on 4 layers (2s2p) FR4 PCB defined in accordance with JESD51-5/ JESD51-7.

Electrical Characteristics (T_J=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=1mA	40	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.2	2.7	3.2	
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	–	0.47	0.61	mΩ
		V_{GS}=7V, I_D=25A	–	0.58	0.76	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	–	–	1	μA
		V_{DS}=40V, V_{GS}=0V, T_J=125°C (4)	–	–	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	–	–	±100	nA
Gate Resistance	R_g	f =1MHz	–	1.9	–	Ω
Transfer characteristics(4)	g_{fs}	V_{DS}=5V, I_D=50A	–	200	–	S
Dynamic Characteristics(4)						
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=1MHz	–	9850	12805	pF
Output Capacitance	C_{oss}		–	2750	3575	
Reverse Transfer Capacitance	C_{rss}		–	190	285	
Output Charge	Q_{oss}	V_{DD}=20V, V_{GS}=0V	–	100	–	nC
Total Gate Charge	Q_g	V_{DD}=20V, I_D=50A, V_{GS}=0~10V	–	140	182	
Gate-Source Charge	Q_{gs}		–	40	52	
Gate-Drain Charge	Q_{gd}		–	21	32	
Threshold Gate Charge	$Q_{g(th)}$		–	26	–	
Switching Charge	Q_{sw}		–	35	–	
Gate Plateau Voltage	$V_{plateau}$		–	4.1	–	V
Total Gate Charge, sync. FET	$Q_{g(sync)}$	V_{DD}=0.1V, I_D=50A, V_{GS}=0~10V	–	119	–	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, I_D=50A, R_G=3Ω	–	20	–	ns
Rise Time	t_r		–	15	–	
Turn-Off Delay Time	$t_{d(off)}$		–	90	–	
Fall Time	t_f		–	40	–	
Body Diode						
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	–	0.8	0.96	V
Reverse Recovery Charge(4)	Q_{rr}	I_S=50A, di/dt=100A/μs	–	55	–	nC
Reverse Recovery Time(4)	T_{rr}		–	45	–	ns

Notes :

(4). Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

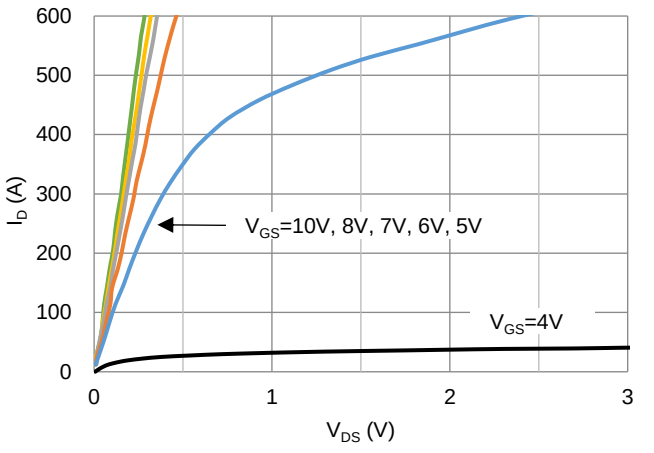


Fig.1 Output Characteristics

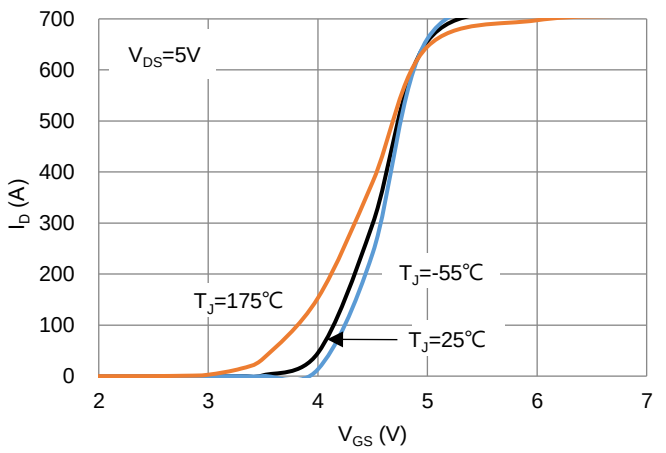


Fig.2 Transfer Characteristics

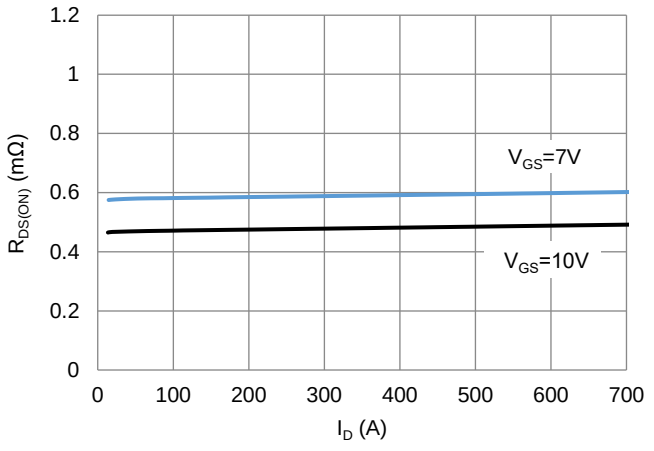


Fig.3 On-Resistance vs. Drain Current

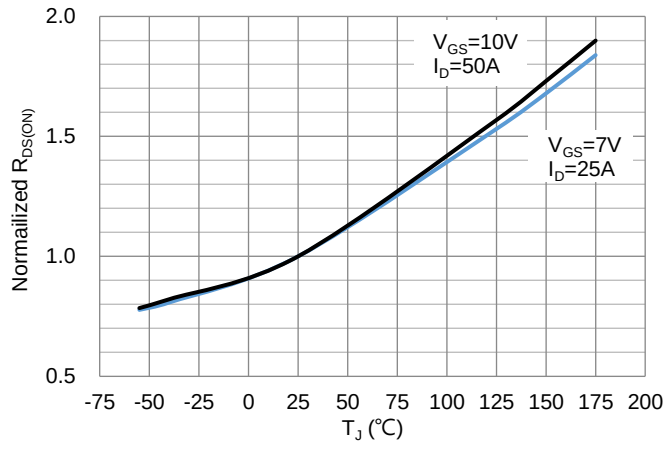


Fig.4 On-Resistance vs. Junction temperature

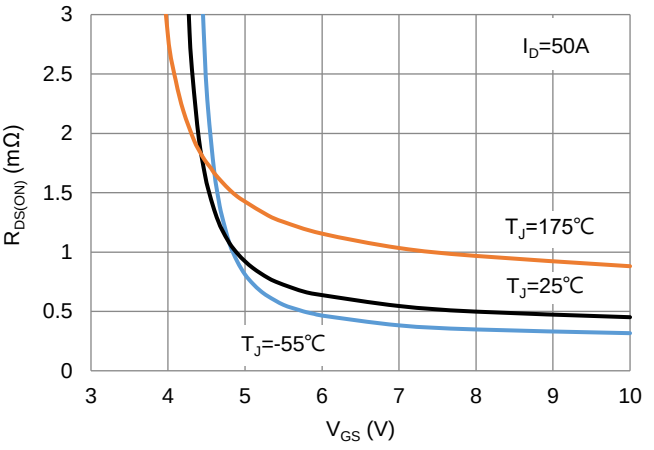


Fig.5 On-Resistance vs. Gate Voltage

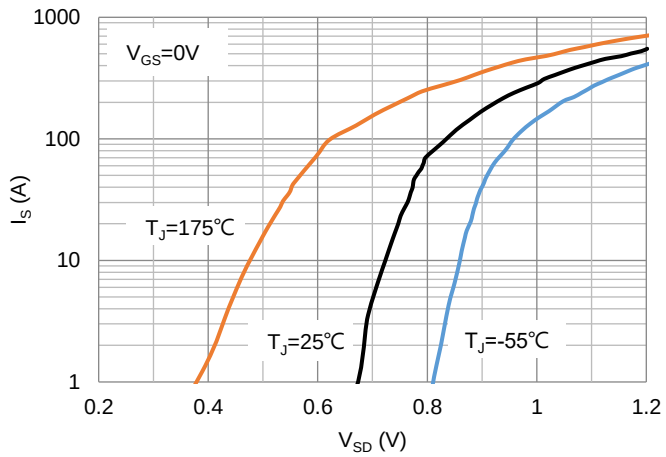


Fig.6 Body Diode Characteristics

TYPICAL CHARACTERISTIC CURVES

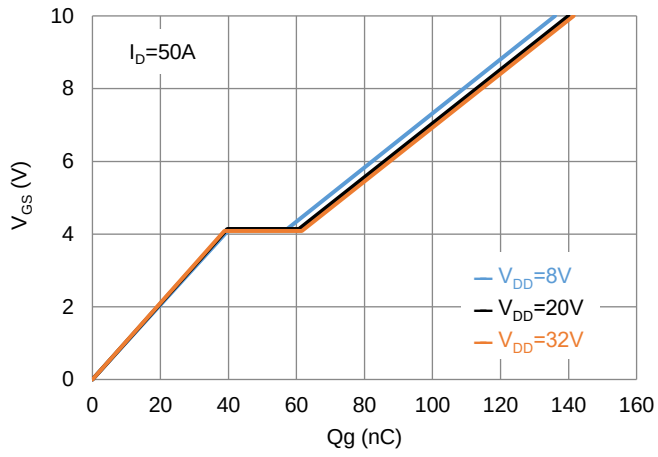


Fig.7 Gate-Charge Characteristics

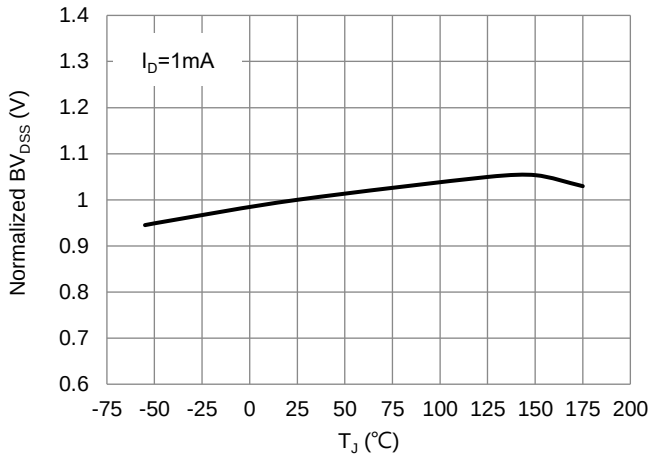


Fig.8 Breakdown Voltage vs. Junction Temperature

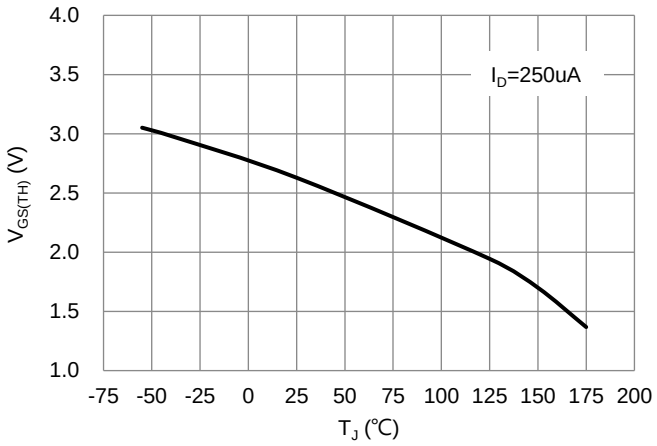


Fig.9 Threshold Voltage vs. Junction Temperature

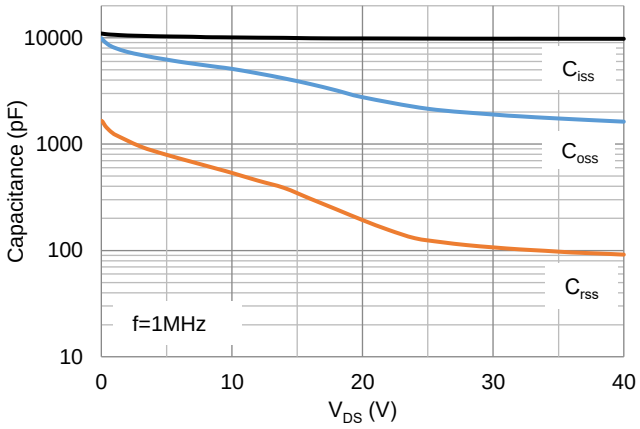


Fig.10 Capacitance vs. Drain-Source Voltage

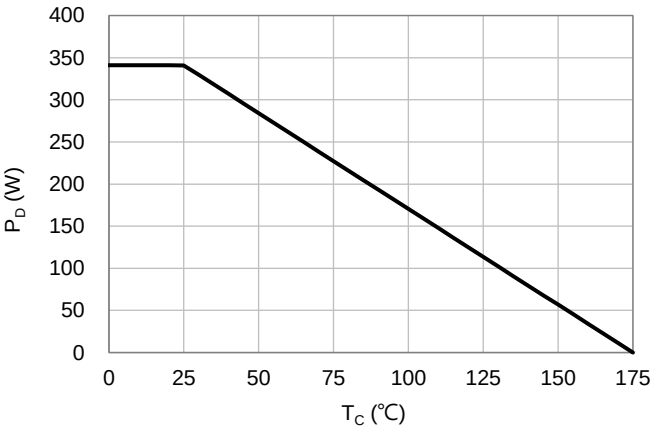


Fig.11 Power Dissipation vs. Case Temperature

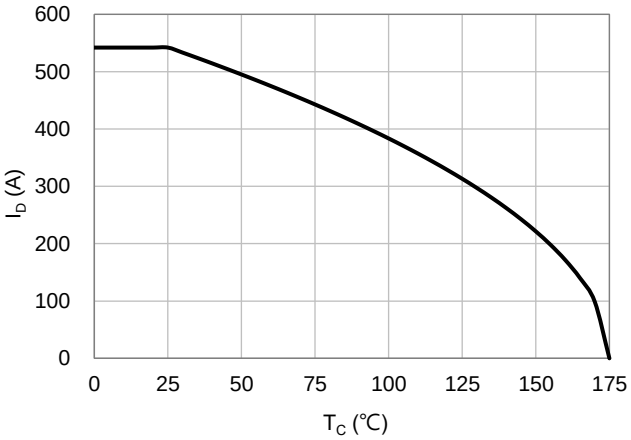


Fig.12 Drain Current vs. Case Temperature

TYPICAL CHARACTERISTIC CURVES

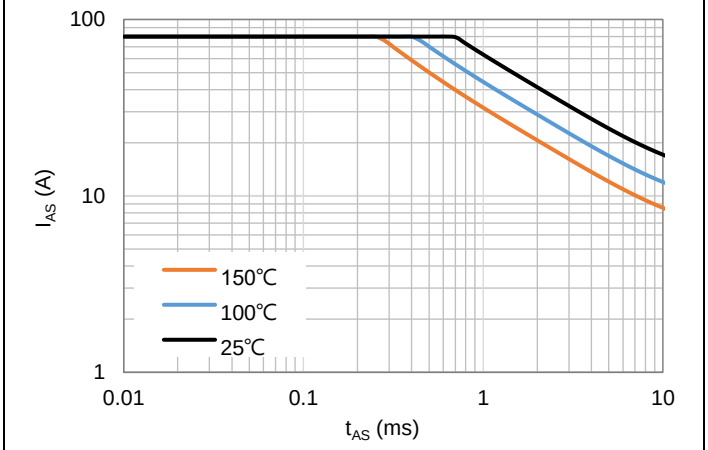


Fig.13 Avalanche characteristics

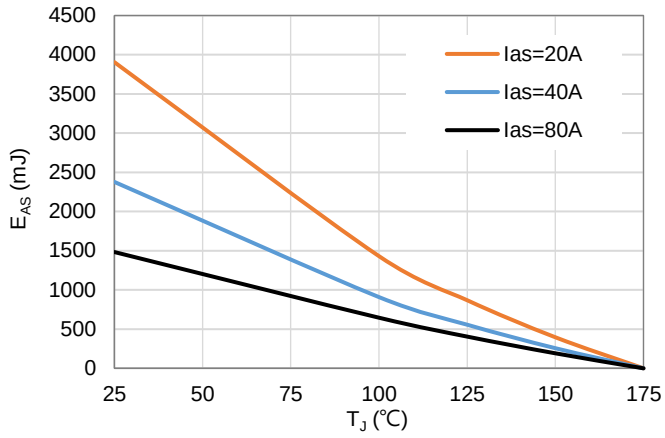


Fig.14 Avalanche Energy

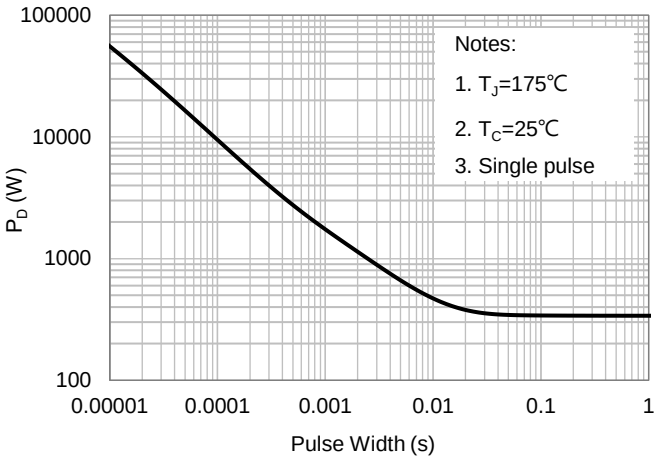


Fig.15 Power Dissipation vs. Pulse Width

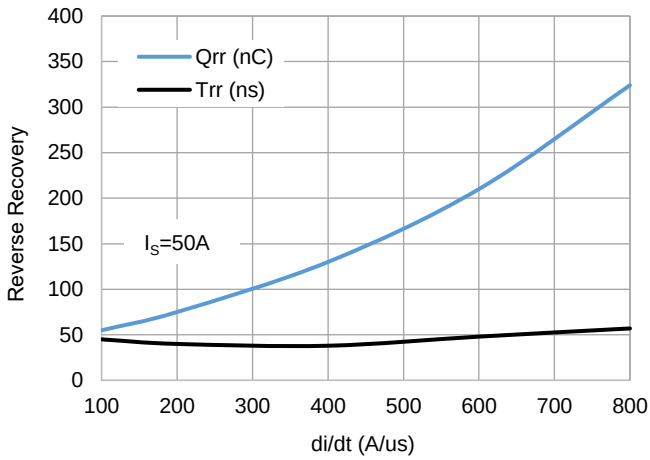


Fig.16 Body Diode Reverse Recovery characteristics

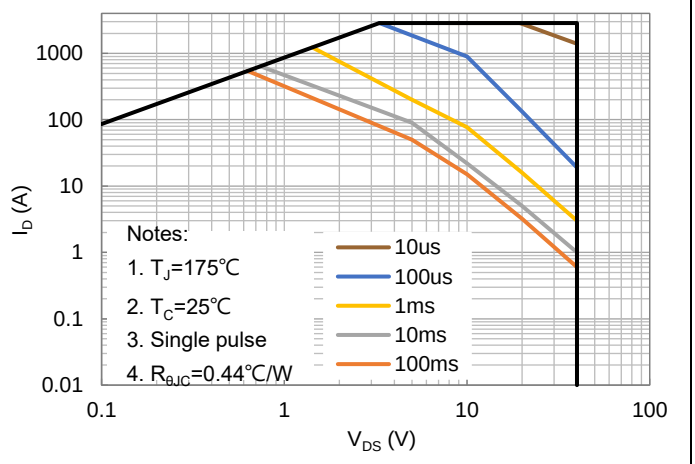


Fig.17 Maximum Safe Operating Area

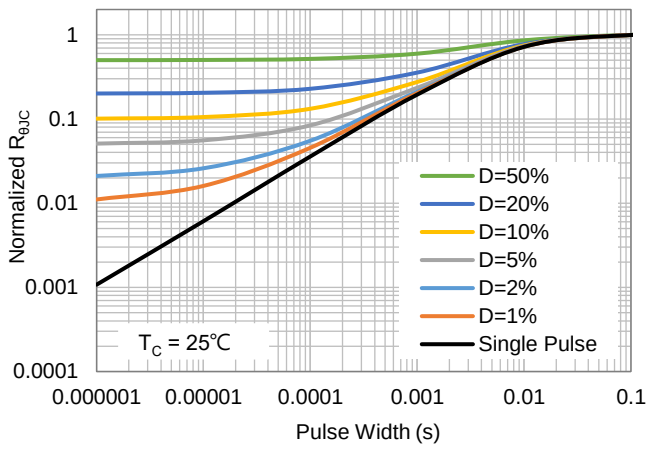


Fig.18 Normalized Thermal Impedance

TEST CIRCUITS AND WAVEFORMS

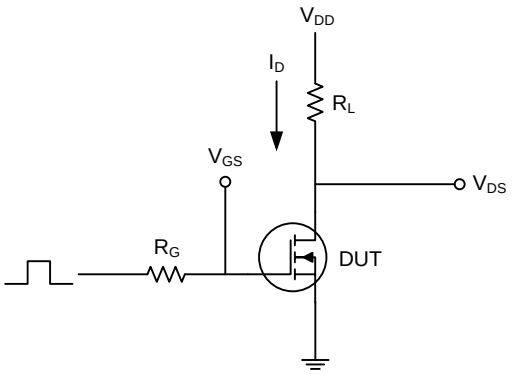


Fig.19 Switching Time Test Circuit

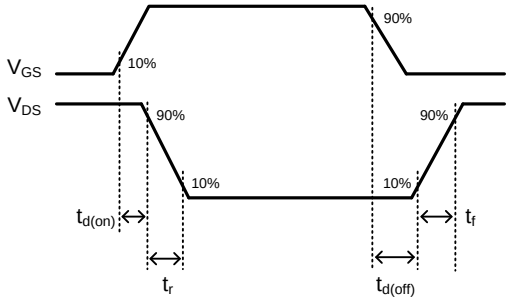


Fig.20 Switching Time Waveform

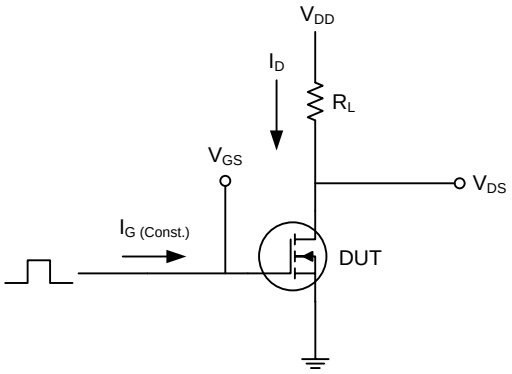


Fig.21 Gate Charge Test Circuit

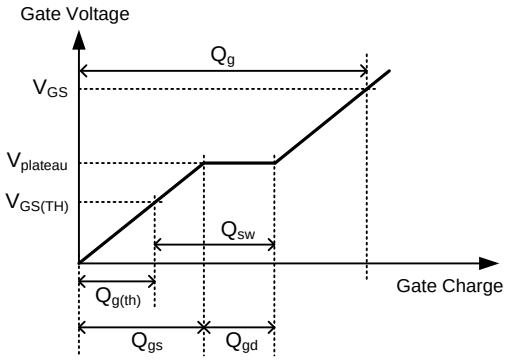


Fig.22 Gate Charge Waveform

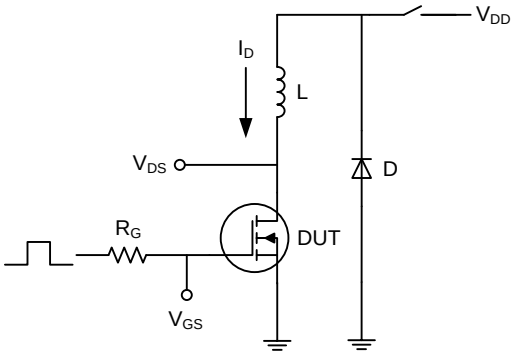
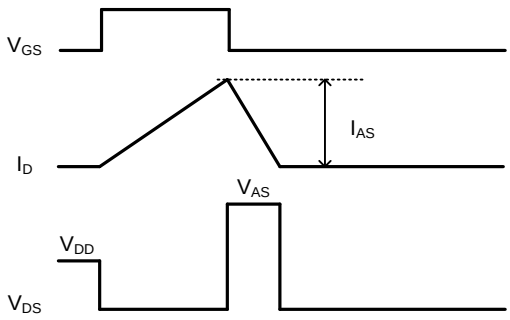


Fig.23 Avalanche Test Circuit



$$E_{AS} = \frac{1}{2} \times L \times {I_{AS}}^2$$

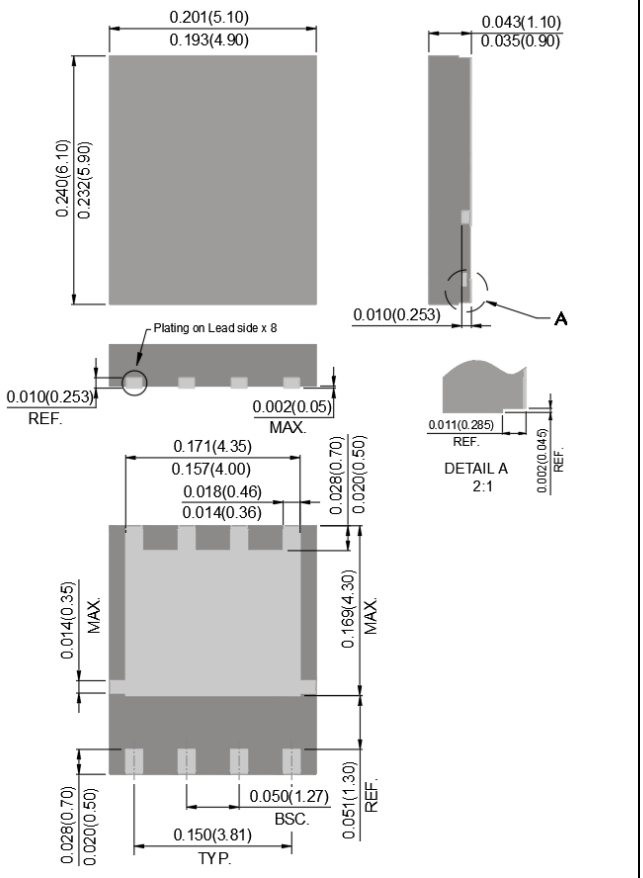
Fig.24 Avalanche Waveform

Product and Packing Information

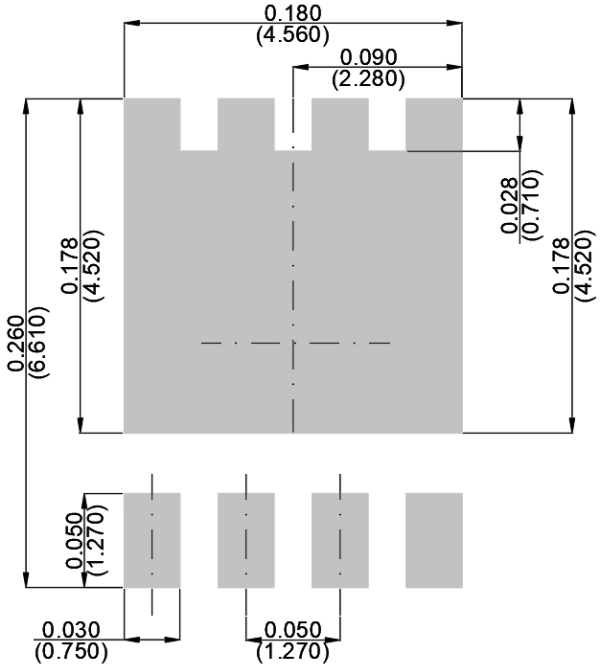
Part No.	Package Type	Packing Type	Marking
PSMWF005N04NS3-AU	DFN5060SW-8L	3K pcs / 13” reel	005N04NS

Packaging & Layout Information

DFN5060SW-8L Dimension — Unit: inch(mm)



DFN5060SW-8L Pad Layout — Unit: inch(mm)



Marking Diagram

PJ **005N04NS** **YWLL x**

Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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