

PJA138K

50V N-Channel Enhancement Mode MOSFET – ESD Protected

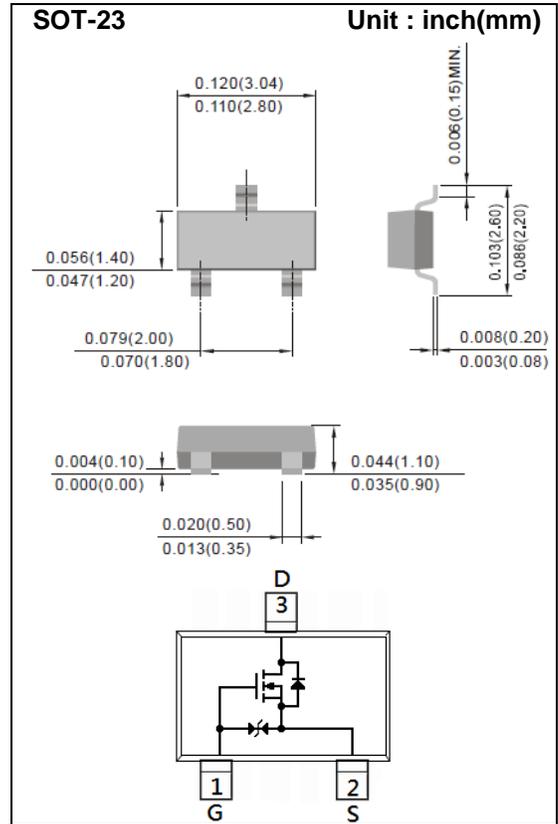
Voltage **50 V** **Current** **500mA**

Features

- RDS(ON) , V_{GS}@10V, I_D@500mA<1.6Ω
- RDS(ON) , V_{GS}@4.5V, I_D@200mA<2.5Ω
- RDS(ON) , V_{GS}@2.5V, I_D@100mA<4.5Ω
- Advanced Trench Process Technology.
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS2.0 (2011/65/EU & 2015/865/EU directive)
- Green molding compound as per IEC61249 Std..(Halogen Free)

Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V _{DS}	50	V	
Gate-Source Voltage	V _{GS}	+20	V	
Continuous Drain Current	I _D	500	mA	
Pulsed Drain Current	I _{DM}	1200	mA	
Power Dissipation	P _D	T _A =25°C	500	mW
		Derate above 25°C	4	mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C	
Typical Thermal Resistance	R _{θJA}	250	°C/W	
- Junction to Ambient (Note 3)				

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	50	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.8	1.0	1.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =500mA	-	0.96	1.6	Ω
		V _{GS} =4.5V, I _D =200mA	-	1.25	2.5	
		V _{GS} =2.5V, I _D =100mA	-	2.73	4.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =50V, V _{GS} =0V	-	0.01	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	±3.0	±10	
Dynamic (Note 4)						
Total Gate Charge	Q _g	V _{DS} =25V, I _D =250mA, V _{GS} =4.5V (Note 1,2)	-	0.63	1	nC
Gate-Source Charge	Q _{gs}		-	0.2	-	
Gate-Drain Charge	Q _{gd}		-	0.23	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	-	25	50	pF
Output Capacitance	C _{oss}		-	9.5	20	
Reverse Transfer Capacitance	C _{rss}		-	2.1	5	
Turn-On Delay Time	t _{d(on)}	V _{DD} =25V, I _D =500mA, V _{GS} =10V, R _G =6Ω (Note 1,2)	-	2.2	5	ns
Turn-On Rise Time	t _r		-	19.2	38	
Turn-Off Delay Time	t _{d(off)}		-	6.2	12	
Turn-Off Fall Time	t _f		-	23	50	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _s	---	-	-	500	mA
Diode Forward Voltage	V _{SD}	I _s =500mA, V _{GS} =0V	-	0.86	1.5	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper
4. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

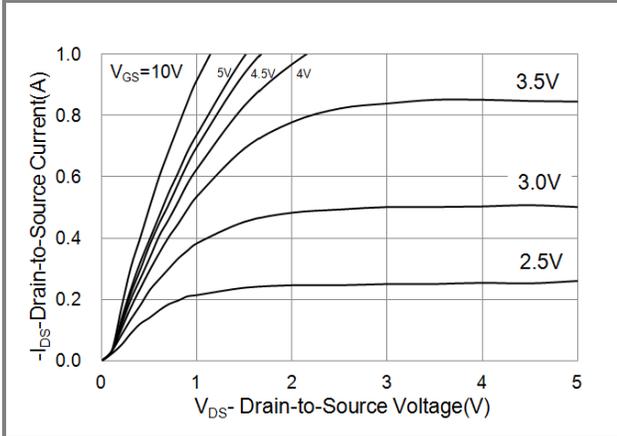


Fig.1 On-Region Characteristics

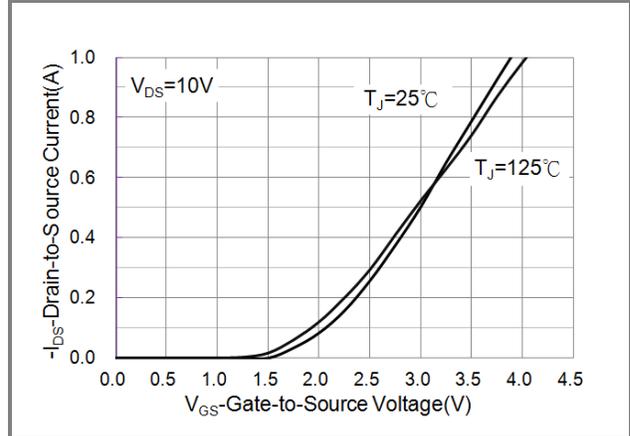


Fig.2 Transfer Characteristics

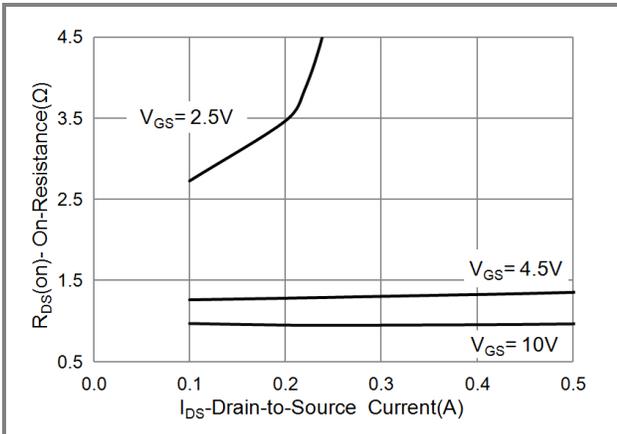


Fig.3 On-Resistance vs. Drain Current

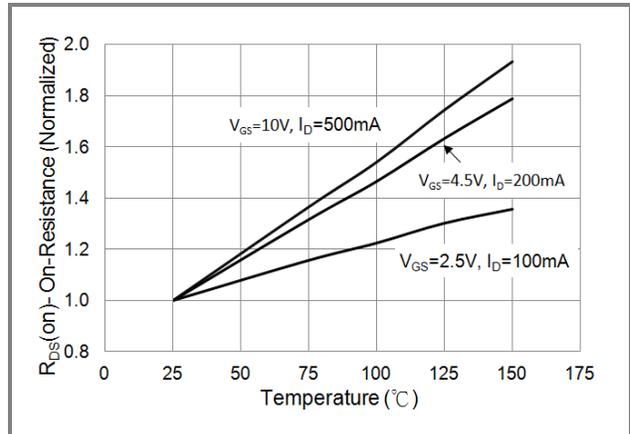


Fig.4 On-Resistance vs. Junction temperature

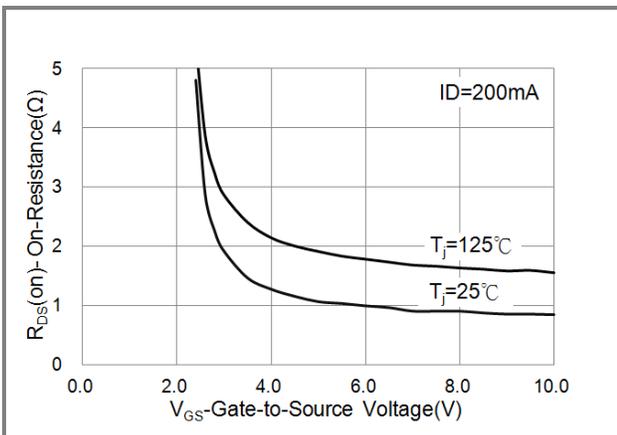


Fig.5 On-Resistance Variation with VGS.

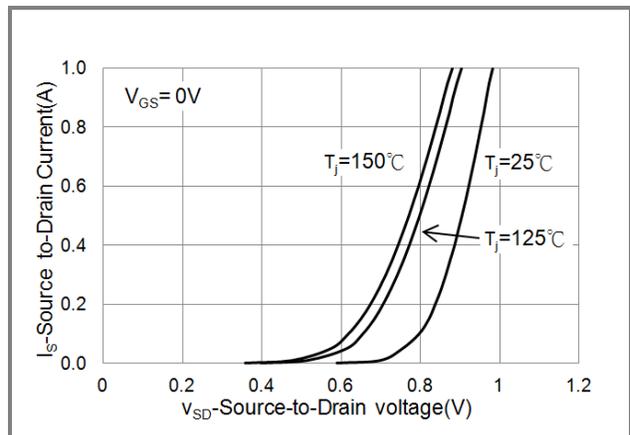


Fig.6 Body Diode Characteristics

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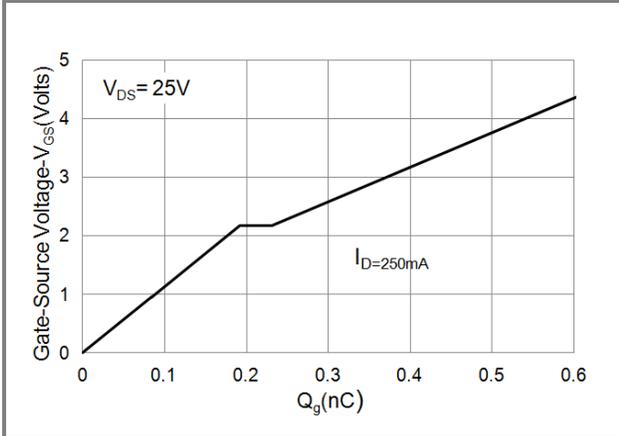


Fig.7 Gate-Charge Characteristics

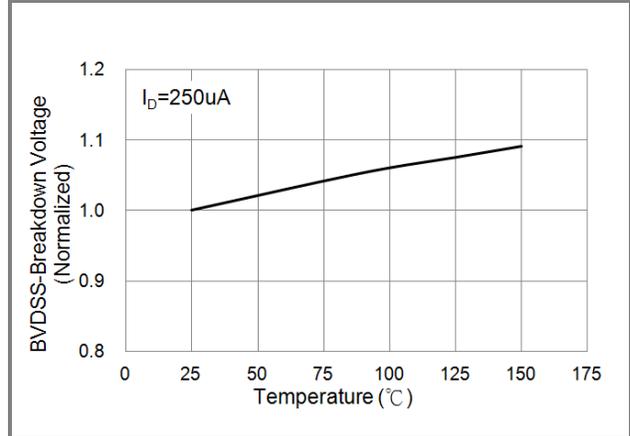


Fig.8 Breakdown Voltage Variation vs. Temperature

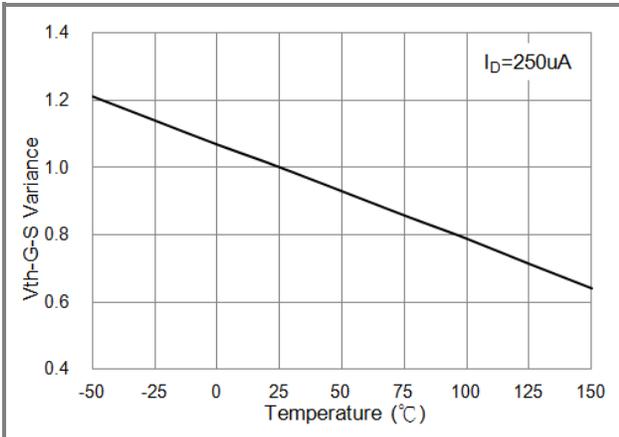


Fig.9 Threshold Voltage Variation with Temperature.

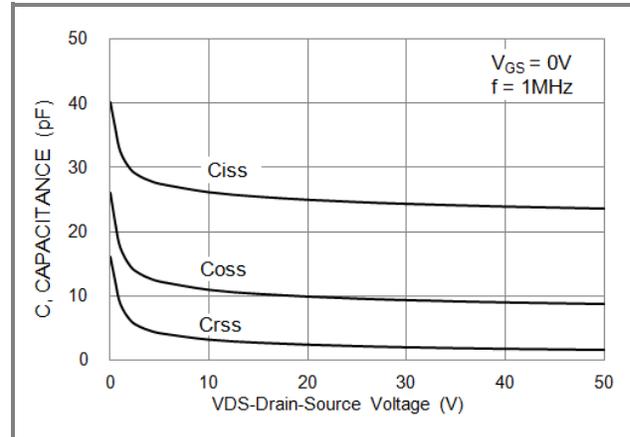


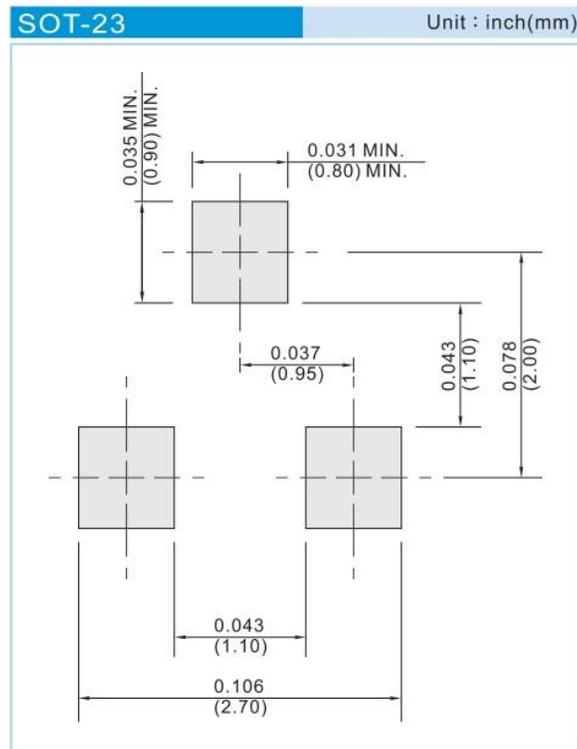
Fig.10 Capacitance vs. Drain-Source Voltage.

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJA138K	SOT-23	3K pcs / 7" reel	8K3
PJA138K	SOT-23	12K pcs / 13" reel	8K3

Mounting Pad Layout



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