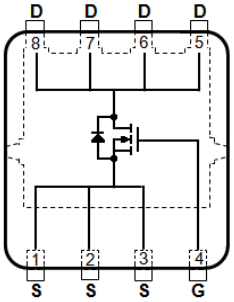
PJQ5572A-AU

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	Current	75 A

DFN5060-8L



Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@20A<7.4mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@10A<11mΩ
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(Note 3)	T_C=25°C	I_D	75	A
	T_C=100°C		53	
Pulsed Drain Current(Note 1)	T_C=25°C	I_{DM}	300	
Power Dissipation	T_C=25°C	P_D	83	W
	T_C=100°C		42	
Continuous Drain Current(Note 4)	T_A=25°C	I_D	15	A
	T_A=70°C		12.6	
Power Dissipation	T_A=25°C	P_D	3.3	W
	T_A=70°C		2.3	
Single Pulse Avalanche Current(Note 5)		I_{AS}	40	A
Single Pulse Avalanche Energy(Note 5)		E_{AS}	85	mJ
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C
Thermal Resistance(Note 4)	Junction to Case	$R_{\theta JC}$	1.8	°C/W
	Junction to Ambient	$R_{\theta JA}$	45	

PJQ5572A-AU

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.5	2.1	3	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	5.9	7.4	mΩ
		V_{GS}=4.5V, I_D=10A	-	8.4	11	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=50V, I_D=20A, V_{GS}=10V	-	62	-	nC
Gate-Source Charge	Q_{gs}		-	11	-	
Gate-Drain Charge	Q_{gd}		-	18	-	
Input Capacitance	Ciss	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	2658	-	pF
Output Capacitance	Coss		-	381	-	
Reverse Transfer Capacitance	Crss		-	24	-	
Gate resistance	R_g	f=1MHz	-	0.9	-	Ω
Turn-On Delay Time	$td_{(on)}$	V_{DS}=50V, I_D=20A, V_{GS}=10V, R_G=3Ω (Note 2)	-	11	-	ns
Turn-On Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$td_{(off)}$		-	52	-	
Turn-Off Fall Time	t_f		-	22	-	
Drain-Source Diode						
Diode Forward Current	I_S	T_C=25°C	-	-	75	A
Pulsed Diode Forward Current	I_{SM}		-	-	300	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	0.85	1.3	V
Reverse Recovery Time	Trr	V_{GS}=0V, I_S=20A dIs/dt=100A/us	-	56	-	ns
Reverse Recovery Charge	Qrr		-	62	-	nC

NOTES :

1. Pulse width≤100us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an $R_{\theta JC}$=1.8°C/W.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch^2 with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=13A, V_{DD}=30V, V_{GS}=10V. 100% test at L=0.1mH, I_{AS}=40A in production.
6. Guaranteed by design, not subject to production testing.

PJQ5572A-AU

TYPICAL CHARACTERISTIC CURVES

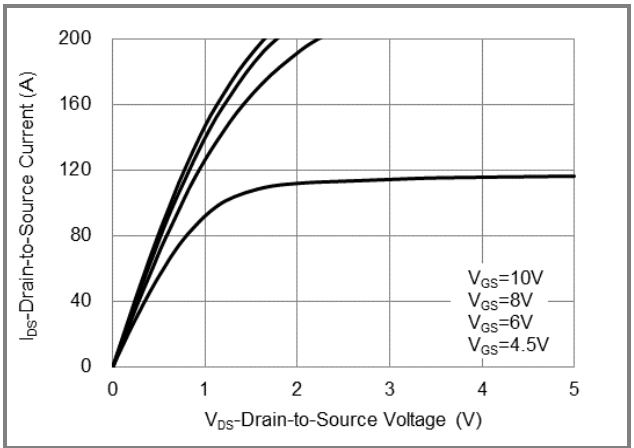


Fig.1 On-Region Characteristics

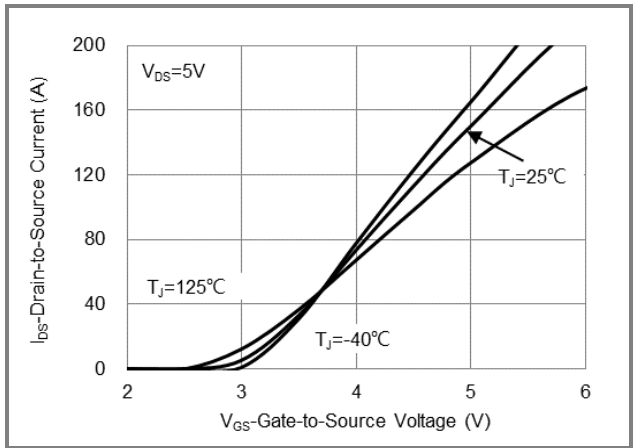


Fig.2 Transfer Characteristics

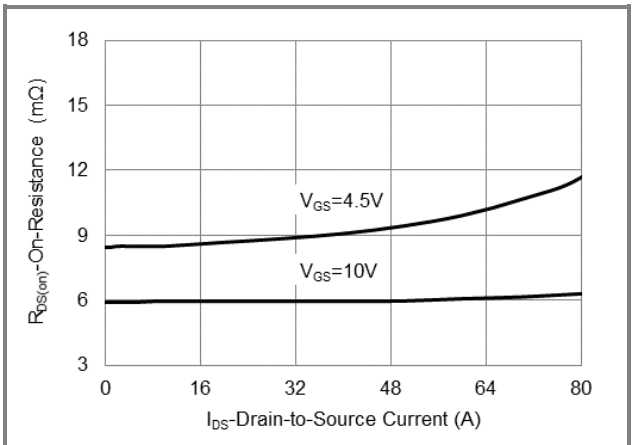


Fig.3 On-Resistance vs. Drain Current

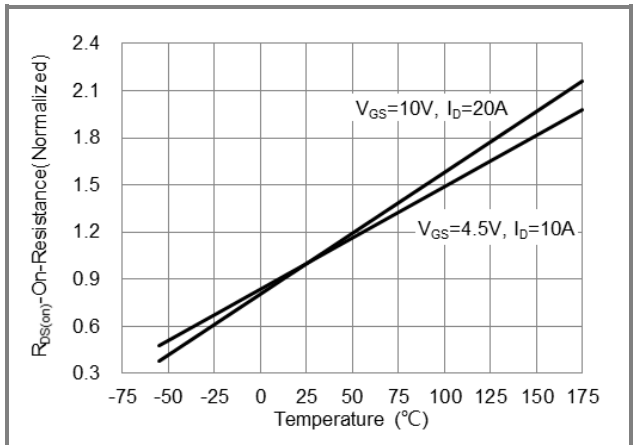


Fig.4 On-Resistance vs. Junction temperature

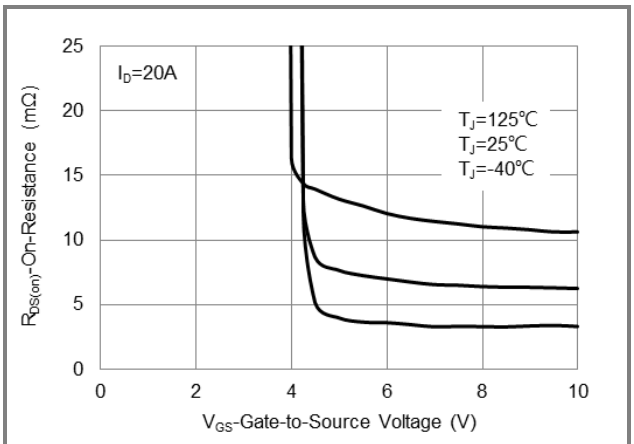


Fig.5 On-Resistance Variation with V_{GS}

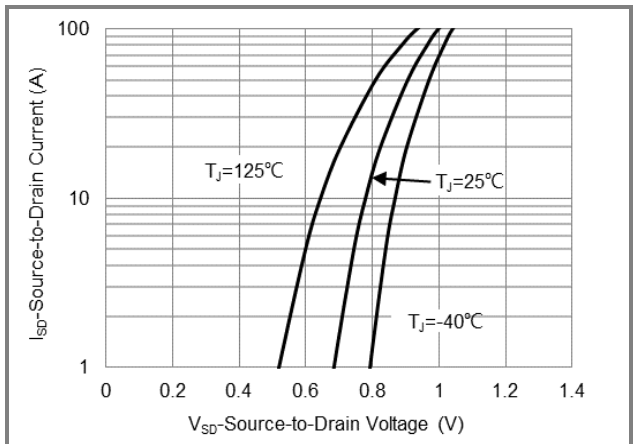


Fig.6 Source-Drain Diode Forward Voltage

PJQ5572A-AU

TYPICAL CHARACTERISTIC CURVES

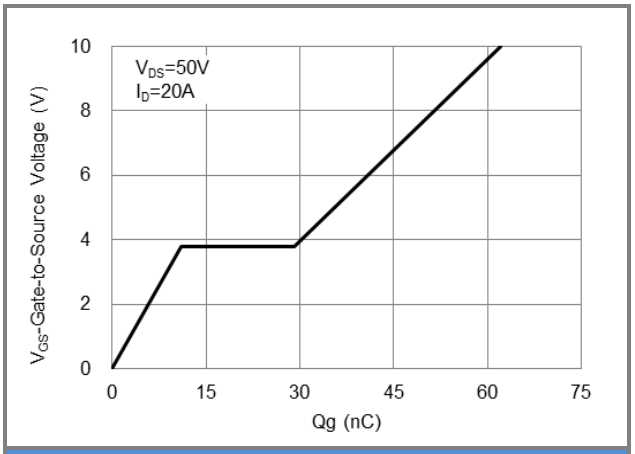


Fig.7 Gate-Charge Characteristics

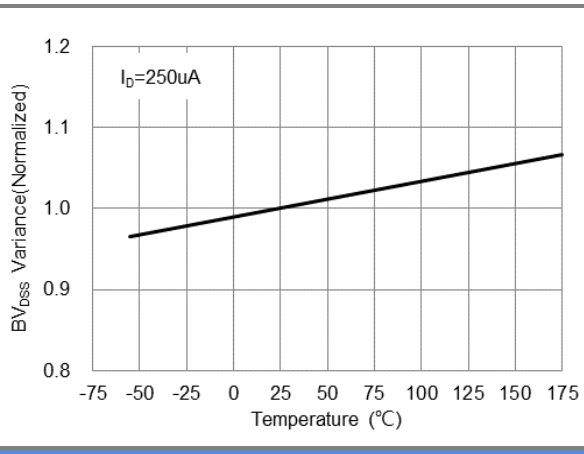


Fig.8 Breakdown Voltage Variation vs. Temperature

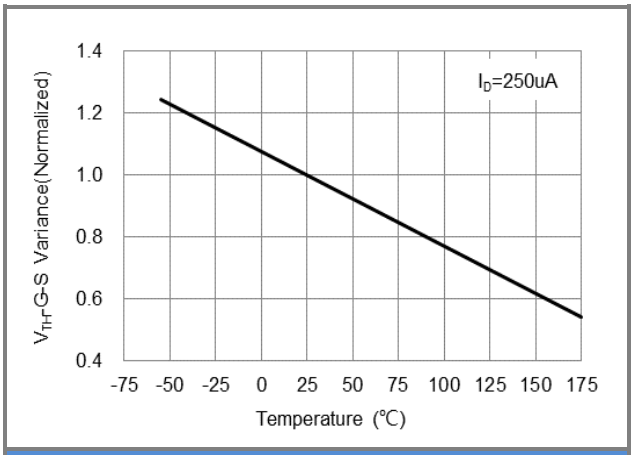


Fig.9 Threshold Voltage Variation with Temperature

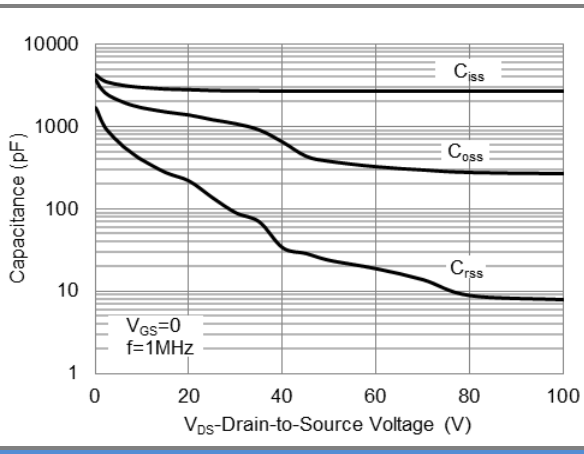


Fig.10 Capacitance vs. Drain-Source Voltage

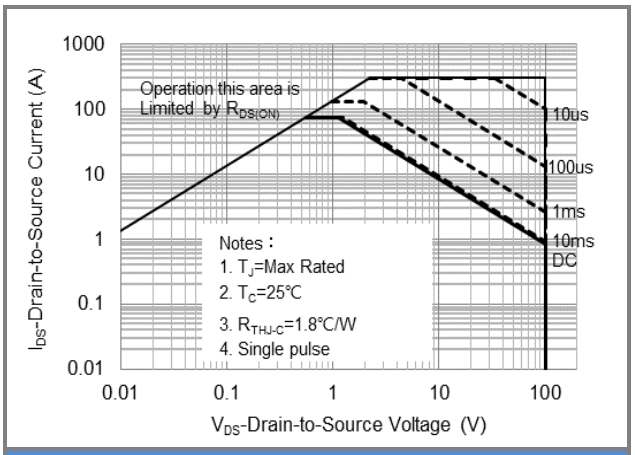


Fig.11 Maximum Safe Operating Area

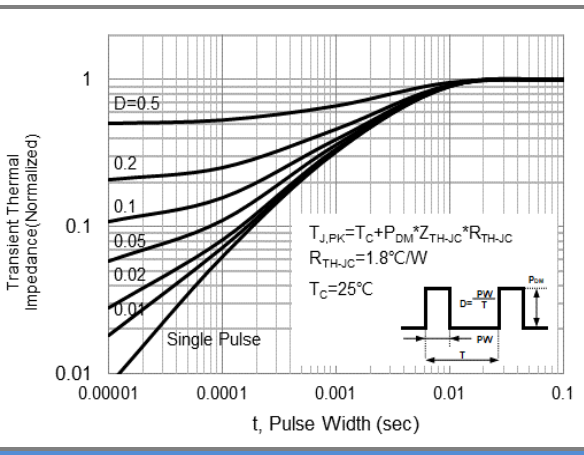


Fig.12 Normalized Transient Thermal Impedance

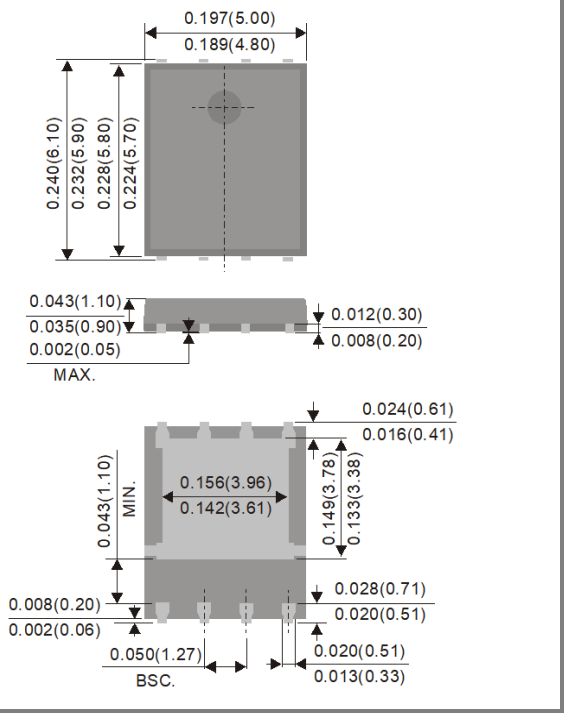
PJQ5572A-AU

Product and Packing Information

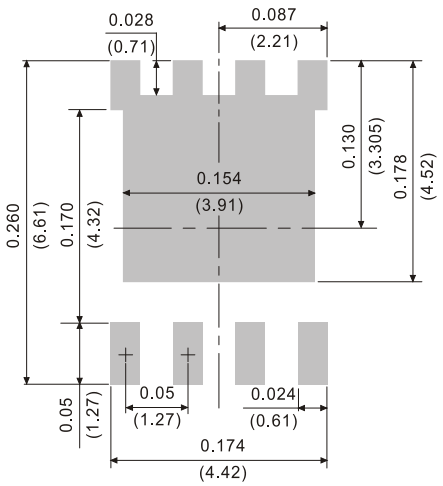
Part No.	Package Type	Packing Type	Marking
PJQ5572A-AU	DFN5060-8L	3K pcs / 13” reel	Q5572A

Packaging Information & Mounting Pad Layout

DFN5060-8L Dimension — Unit: inch(mm)



DFN5060-8L Pad Layout — Unit: inch(mm)



Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from Panjit International Inc..
- Panjit International Inc. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- Panjit International Inc. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- Panjit International Inc. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. Panjit International Inc. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panjit International Inc. for any damages resulting from such improper use or sale.
- Since Panjit uses lot number as the tracking base, please provide the lot number for tracking when complaining.