

PJQ4441P-AU

40V P-Channel Enhancement Mode MOSFET

Voltage **-40 V** **Current** **-44 A**

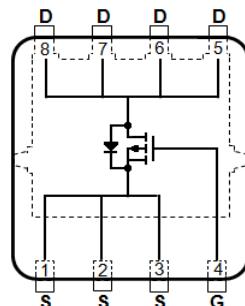
Features

- $R_{DS(ON)}$, $V_{GS} @ -10V$, $I_D @ -10A < 17m\Omega$
- $R_{DS(ON)}$, $V_{GS} @ -4.5V$, $I_D @ -8A < 25m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultralow on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	I_D	-44	A
		-28	
Pulsed Drain Current ^(Note 1)	I_{DM}	-135	W
Power Dissipation	P_D	59.5	
		24	
Continuous Drain Current ^(Note 4)	I_D	-8.5	A
		-7	
Power Dissipation	P_D	2	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	°C
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	$R_{\theta JC}$	2.1
	Junction to Ambient	$R_{\theta JA}$	62.5

- Limited only By Maximum Junction Temperature

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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

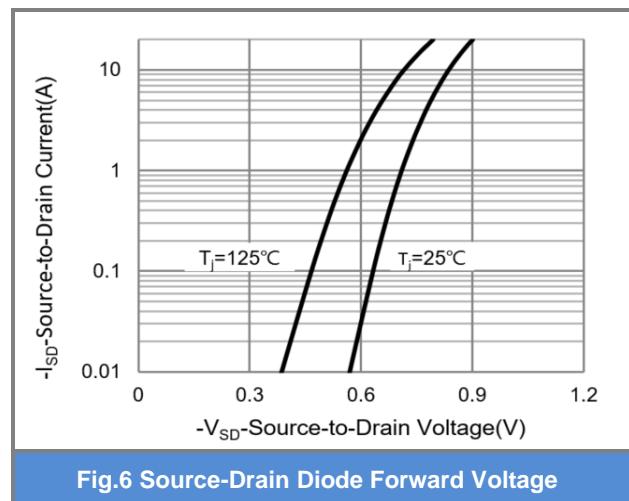
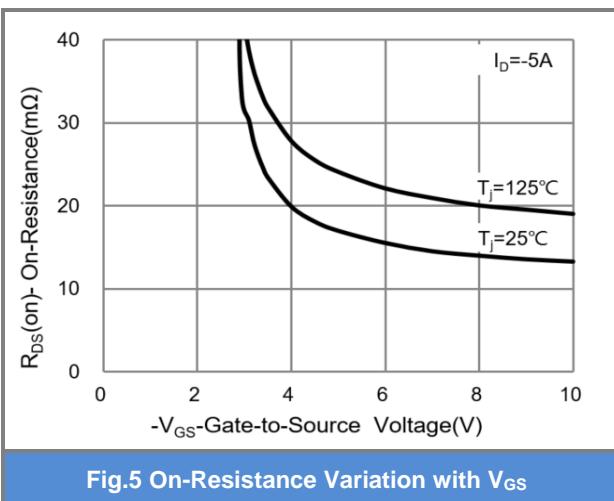
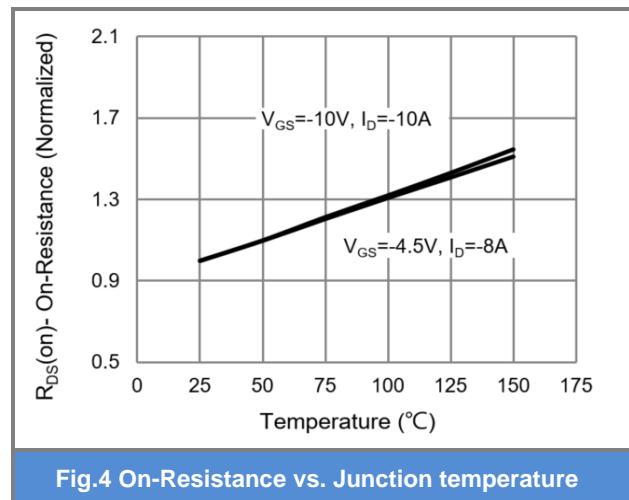
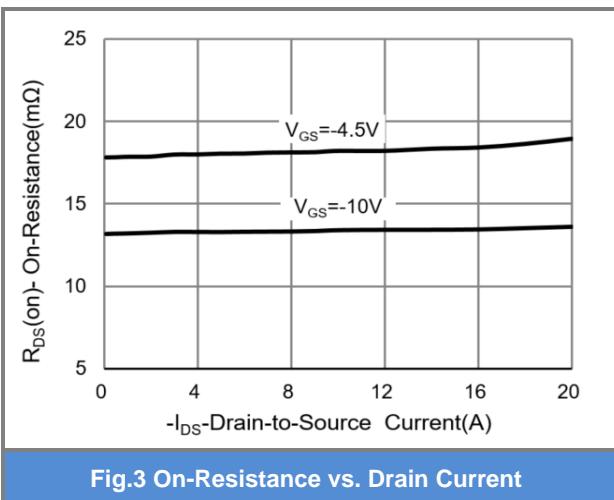
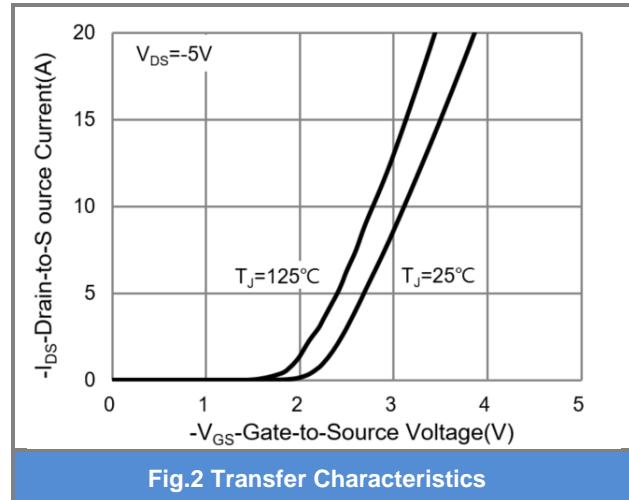
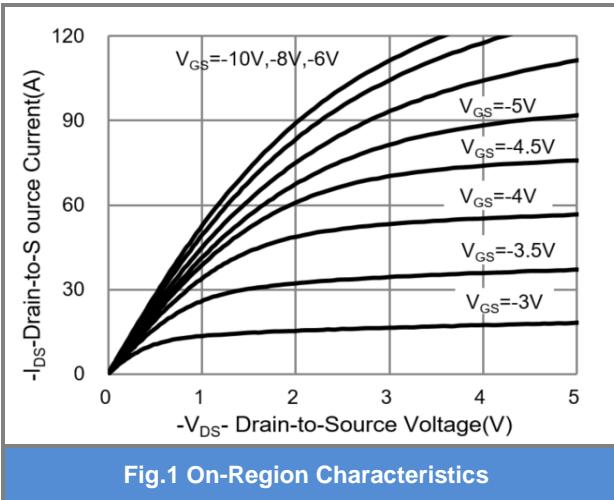
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=-250\mu\text{A}$	-40	-	-	V
Gate Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=-250\mu\text{A}$	-1	-1.6	-2.5	
Drain-Source On-State Resistance	$\text{R}_{\text{DS}(\text{on})}$	$\text{V}_{\text{GS}}=-10\text{V}, \text{I}_D=-10\text{A}$	-	14	17	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=-4.5\text{V}, \text{I}_D=-8\text{A}$	-	20	25	
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=-40\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=-32\text{V}, \text{I}_D=-10\text{A}, \text{V}_{\text{GS}}=-4.5\text{V}$ ^(Note 1,2)	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	5.3	-	
Gate-Drain Charge	Q_{gd}		-	6.6	-	
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=-25\text{V}, \text{V}_{\text{GS}}=0\text{V}, f=1\text{MHZ}$	-	2030	-	pF
Output Capacitance	C_{oss}		-	190	-	
Reverse Transfer Capacitance	Crss		-	139	-	
Turn-On Delay Time	$\text{t}_{\text{d}(\text{on})}$	$\text{V}_{\text{DS}}=-20\text{V}, \text{I}_D=-1\text{A}, \text{V}_{\text{GS}}=-10\text{V}, \text{R}_G=6\Omega$ ^(Note 1,2)	-	8.6	-	ns
Turn-On Rise Time	t_r		-	9.6	-	
Turn-Off Delay Time	$\text{t}_{\text{d}(\text{off})}$		-	77	-	
Turn-Off Fall Time	t_f		-	39	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	-44	A
Diode Forward Voltage	V_{SD}	$\text{I}_s=-1\text{A}, \text{V}_{\text{GS}}=0\text{V}$	-	-0.7	-1	V

NOTES :

1. Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $\text{T}_{\text{J}(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $\text{T}_j = 25^\circ\text{C}$.
4. The maximum current rating is package limited.
5. R_{QJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

PJQ4441P-AU

TYPICAL CHARACTERISTIC CURVES



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TYPICAL CHARACTERISTIC CURVES

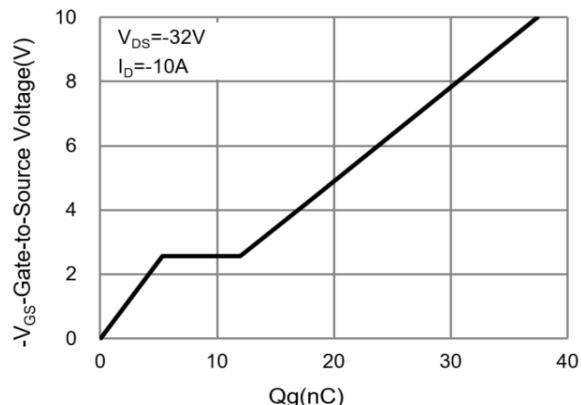


Fig.7 Gate-Charge Characteristics

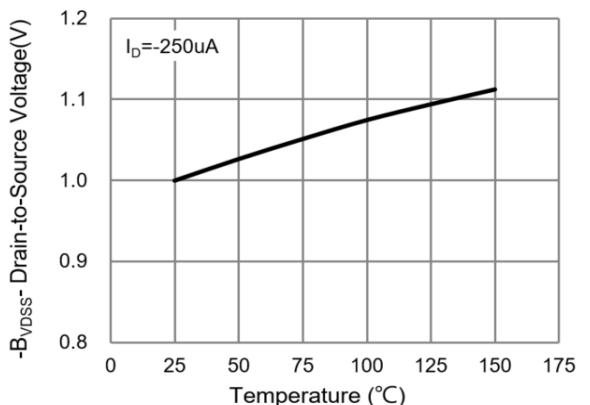


Fig.8 Breakdown Voltage Variation vs. Temperature

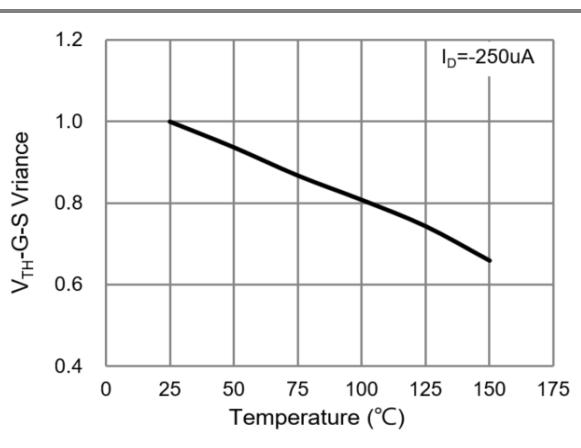


Fig.9 Threshold Voltage Variation with Temperature

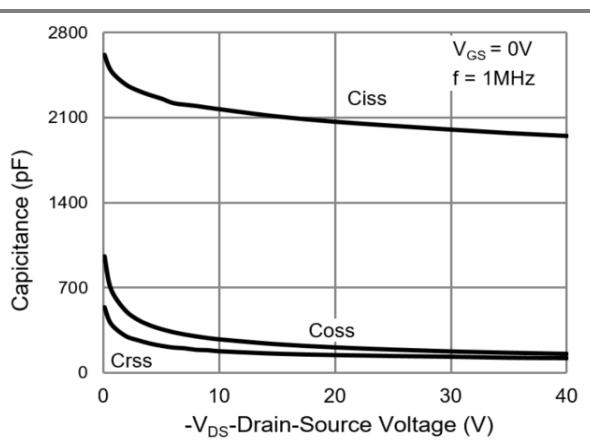


Fig.10 Capacitance vs. Drain-Source Voltage

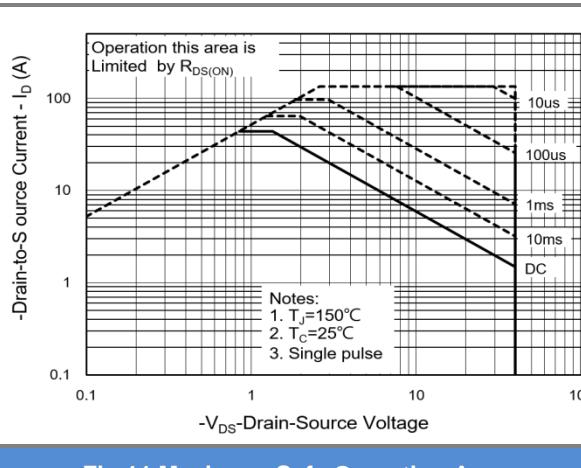


Fig.11 Maximum Safe Operating Area

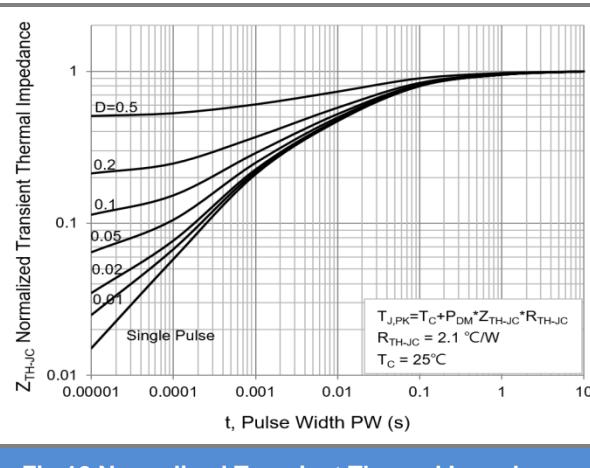


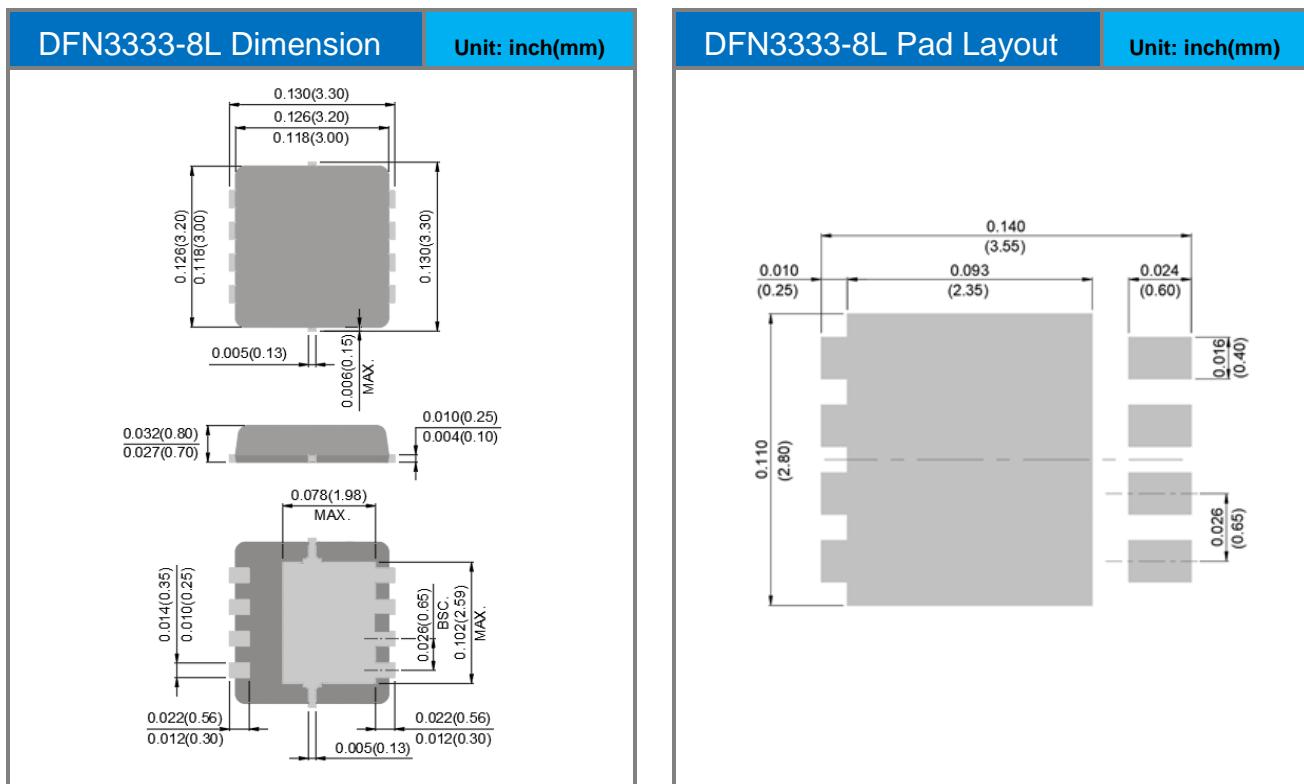
Fig.12 Normalized Transient Thermal Impedance

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ4441P-AU	DFN3333-8L	5K pcs / 13" reel	4441

Packaging Information & Mounting Pad Layout



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