

PJD50P04-AU

40V P-Channel Enhancement Mode MOSFET

Voltage

-40 V

Current

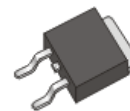
-50 A

Features

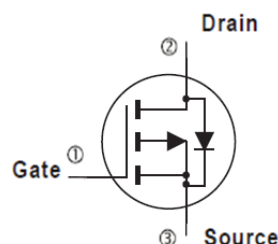
- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-10A < 12m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-8A < 17.5m\Omega$
- High switching speed
- Improved dv/dt capability
- Low gate charge
- Low reverse transfer capacitance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : TO-252AA Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0104 ounces, 0.297grams



TO-252AA



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 4)	$T_C=25^\circ\text{C}$	I_D	-50	A
	$T_C=100^\circ\text{C}$		-32	
Pulsed Drain Current (Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	-166	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	75	W
	$T_C=100^\circ\text{C}$		38	
Continuous Drain Current (Note 4)	$T_A=25^\circ\text{C}$	I_D	-9	A
	$T_A=70^\circ\text{C}$		-7	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.4	W
	$T_A=70^\circ\text{C}$		1.7	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.52	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-10A	-	10	12	mΩ
		V _{GS} =-4.5V, I _D =-8A	-	13.5	17.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =-32V, I _D =-10A, V _{GS} =-4.5V (Note 2,3)	-	23	-	nC
Gate-Source Charge	Q _{gs}		-	8.5	-	
Gate-Drain Charge	Q _{gd}		-	9	-	
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, f=1MHZ	-	2767	-	pF
Output Capacitance	C _{oss}		-	247	-	
Reverse Transfer Capacitance	C _{rss}		-	139	-	
Turn-On Delay Time	td _(on)	V _{DS} =-20V, I _D =-1A, V _{GS} =-10V, R _G =6Ω (Note 2,3)	-	23	-	ns
Turn-On Rise Time	tr		-	10	-	
Turn-Off Delay Time	td _(off)		-	135	-	
Turn-Off Fall Time	tf		-	50	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	Is	---	-	-	-50	A
Diode Forward Voltage	V _{SD}	Is=-1A, V _{GS} =0V	-	-0.7	-1	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J = 25°C.
4. The maximum current rating is package limited.
5. R_{ΘJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

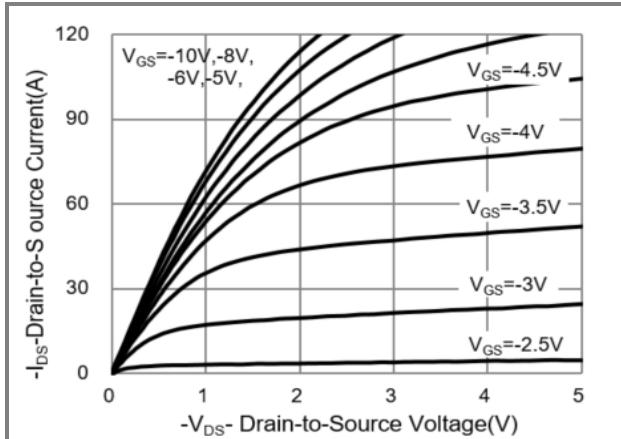


Fig.1 On-Region Characteristics

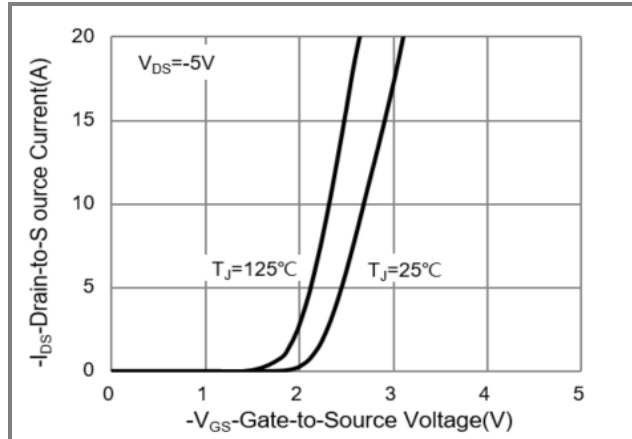


Fig.2 Transfer Characteristics

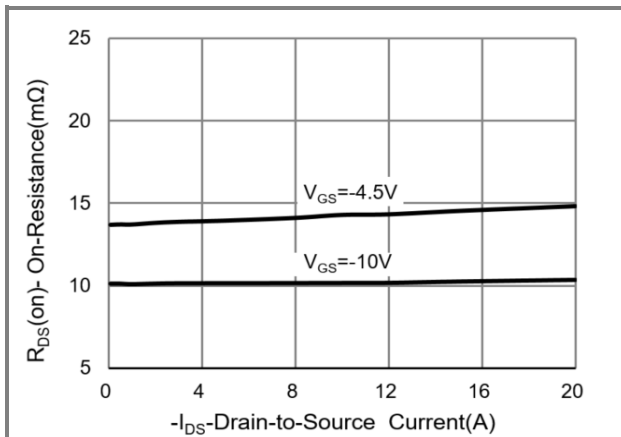


Fig.3 On-Resistance vs. Drain Current

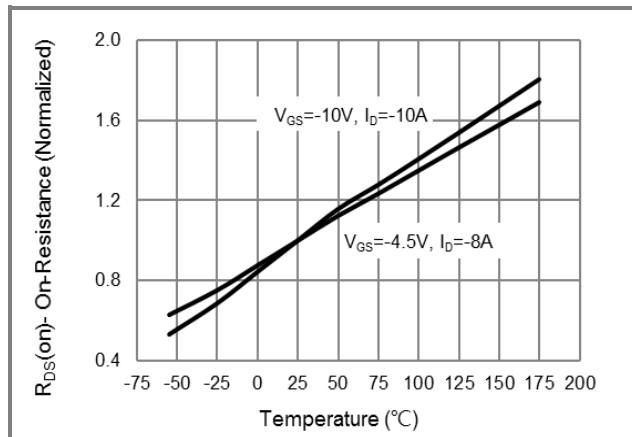


Fig.4 On-Resistance vs. Junction temperature

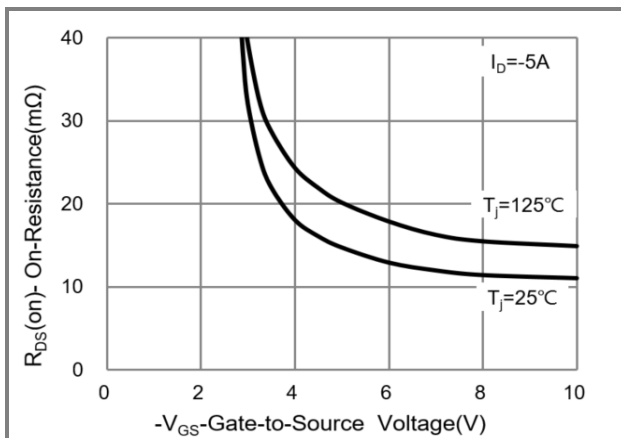


Fig.5 On-Resistance Variation with V_{GS}

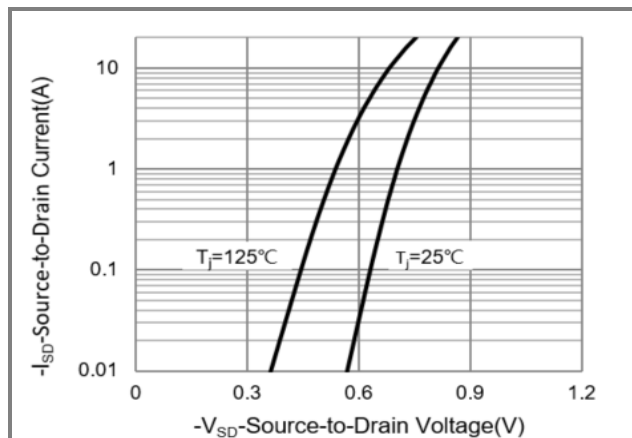
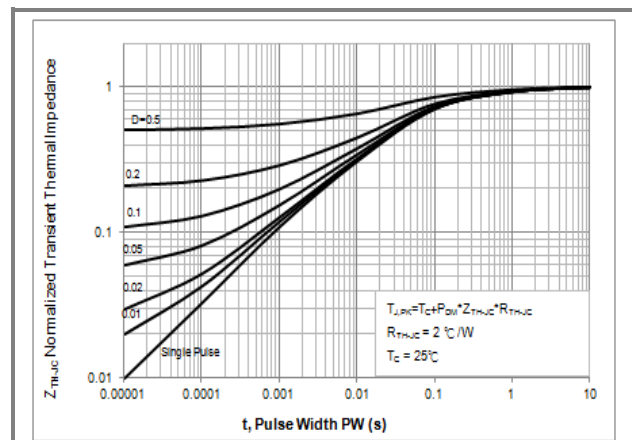
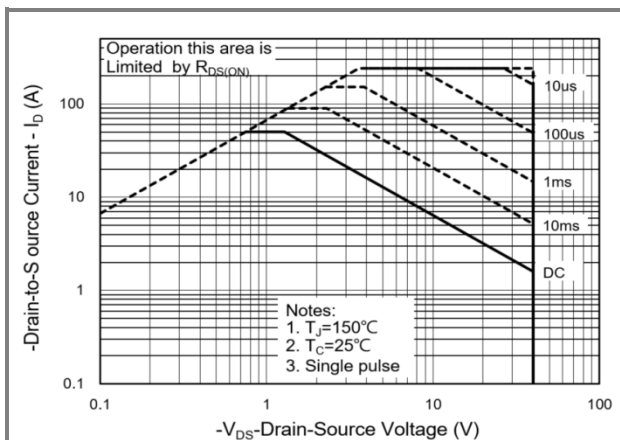
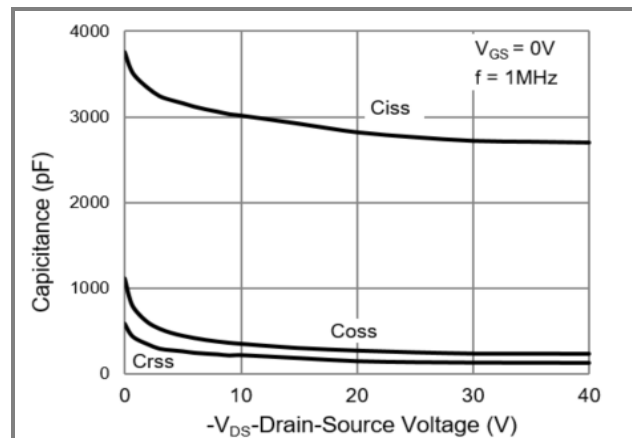
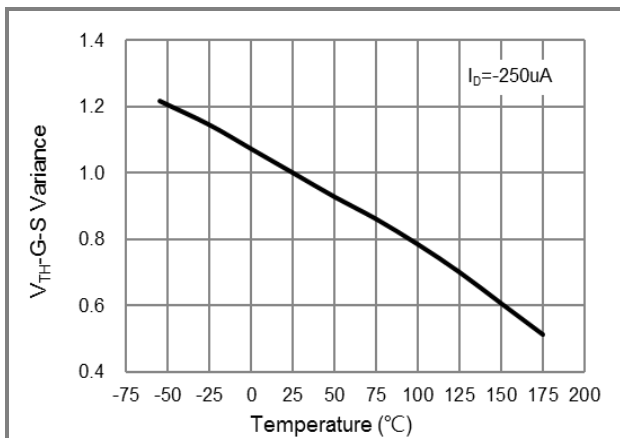
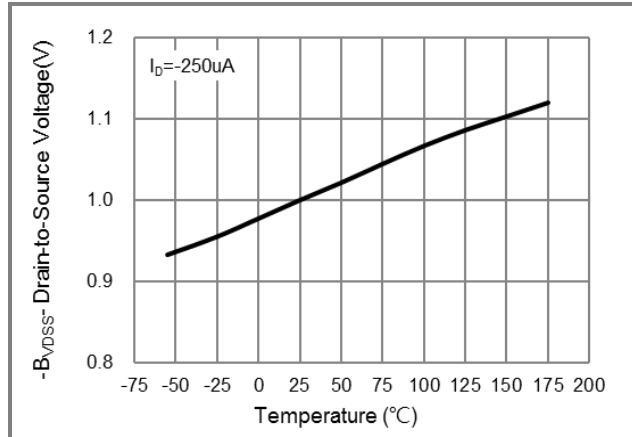
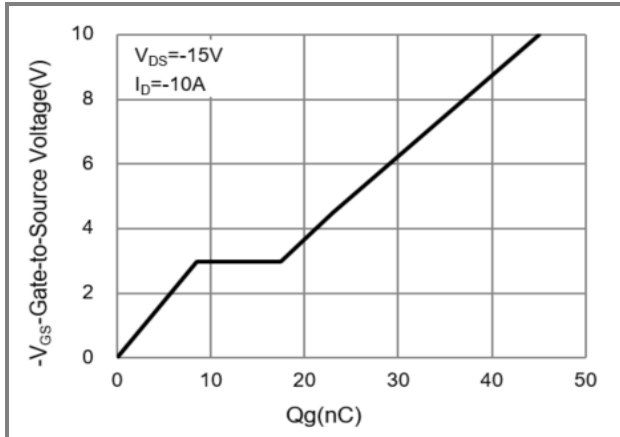


Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

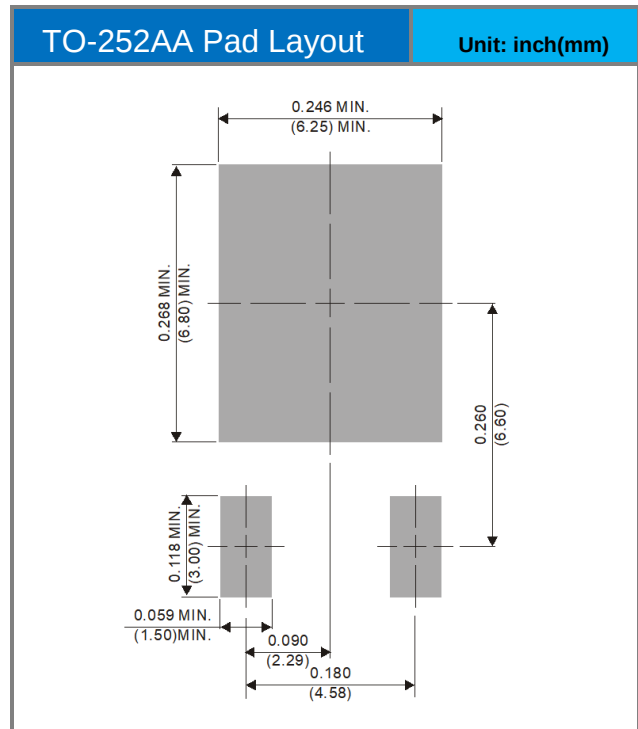
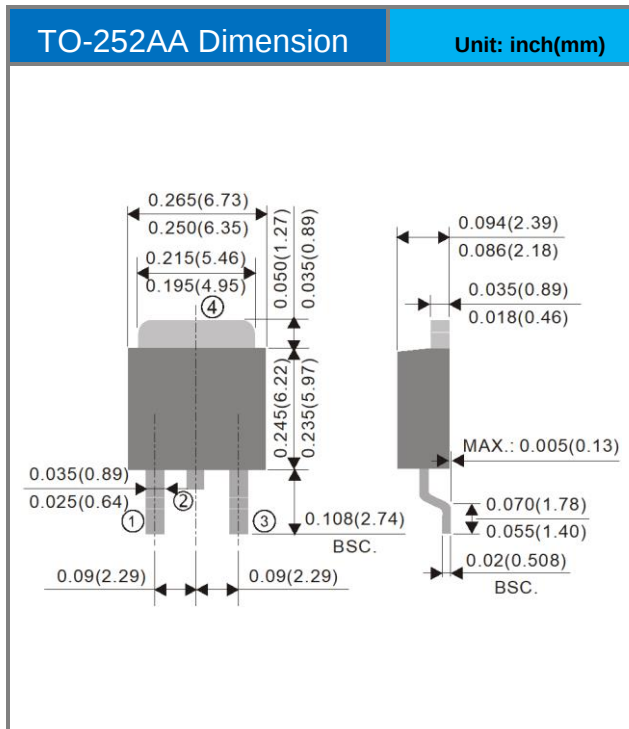


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJD50P04-AU	TO-252AA	3,000pcs / 13" reel	D50P04

Packaging Information & Mounting Pad Layout



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