

PJX8603-AU

Complementary Enhancement Mode MOSFET – ESD Protected

Voltage

50 / -60V

Current

0.36A / -0.2A

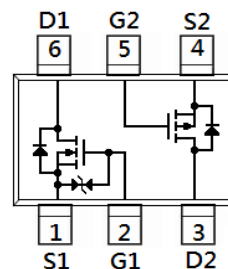
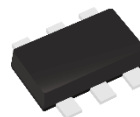
SOT-563

Features

- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- ESD Protected 2KV HBM
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC61249 standard

Mechanical Data

- Case : SOT-563 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0026 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage		V _{DS}	50	-60	V
Gate-Source Voltage		V _{GS}	+20	+20	
Continuous Drain Current ^(Note 4)		I _D	360	-200	mA
Pulsed Drain Current ^(Note 1)		I _{DM}	1200	-900	
Power Dissipation	T _a =25°C	P _D	300		mW
	Derate above 25°C		2.4		mW/°C
Operating Junction and Storage Temperature Range		T _J ,T _{STG}	-55~150		°C
Typical Thermal Resistance		R _{θJA}	417		°C/W
- Junction to Ambient ^(Note 3,4)					

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N-Channel Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D = 250uA	50	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = 250uA	0.5	0.9	1	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 500mA	-	1.26	1.5	Ω
		V _{GS} = 4.5V, I _D = 200mA	-	1.34	2.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±10	
Dynamic ^(Note 5)						
Total Gate Charge	Q _g	V _{DS} =25V, I _D =500mA, V _{GS} =4.5V	-	0.95	-	nC
Gate-Source Charge	Q _{gs}		-	0.34	-	
Gate-Drain Charge	Q _{gd}		-	0.32	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHZ	-	36	-	pF
Output Capacitance	C _{oss}		-	11	-	
Reverse Transfer Capacitance	C _{rss}		-	6.6	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =25V, I _D =500mA, V _{GS} =10V, R _G =6Ω ^(Note 1,2)	-	2.3	-	ns
Turn-On Rise Time	t _r		-	20	-	
Turn-Off Delay Time	t _{d(off)}		-	7	-	
Turn-Off Fall Time	t _f		-	20	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	360	mA
Diode Forward Voltage	V _{SD}	I _S = 500mA, V _{GS} =0V	-	0.9	1.5	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.

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P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.5	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-500mA	-	2.6	6	Ω
		V _{GS} =-4.5V, I _D =-200mA	-	2.9	7	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-48V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =+20V, V _{DS} =0V	-	-	+100	nA
Dynamic ^(Note 5)						
Total Gate Charge	Q _g	V _{DS} =-25V, I _D =-100mA, V _{GS} =-4.5V	-	1.1	-	nC
Gate-Source Charge	Q _{gs}		-	0.3	-	
Gate-Drain Charge	Q _{gd}		-	0.2	-	
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, f=1MHZ	-	51	-	pF
Output Capacitance	C _{oss}		-	15	-	
Reverse Transfer Capacitance	C _{rss}		-	2.2	-	
Turn-On Delay Time	td _(on)	V _{DD} =-25V, I _D =-100mA, V _{GS} =-10V, R _G =6Ω ^(Note 1,2)	-	4.8	-	ns
Turn-On Rise Time	tr		-	19	-	
Turn-Off Delay Time	td _(off)		-	52	-	
Turn-Off Fall Time	tf		-	32	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-200	mA
Diode Forward Voltage	V _{SD}	I _S =-500mA, V _{GS} =0V	-	-0.9	-1.5	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
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N-Channel TYPICAL CHARACTERISTIC CURVES

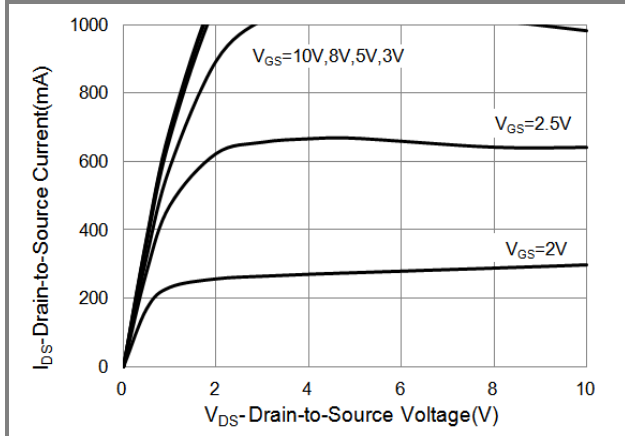


Fig.1 On-Region Characteristics

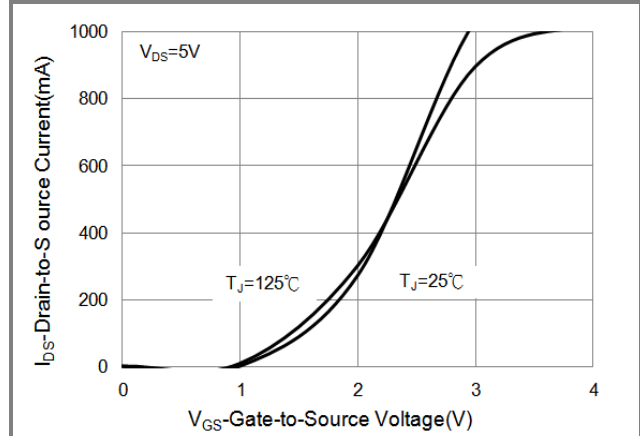


Fig.2 Transfer Characteristics

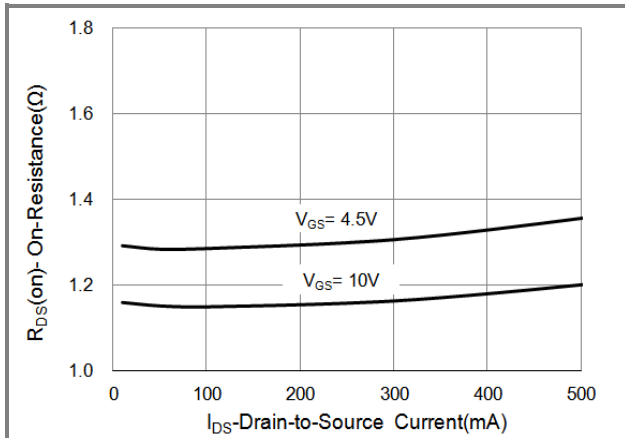


Fig.3 On-Resistance vs. Drain Current

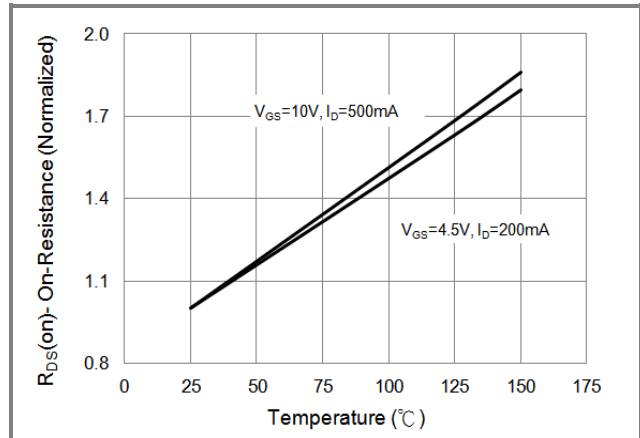


Fig.4 On-Resistance vs. Junction temperature

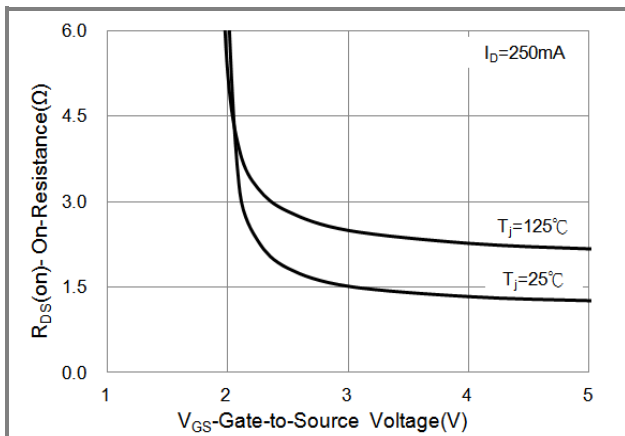


Fig.5 On-Resistance Variation with V_{GS}

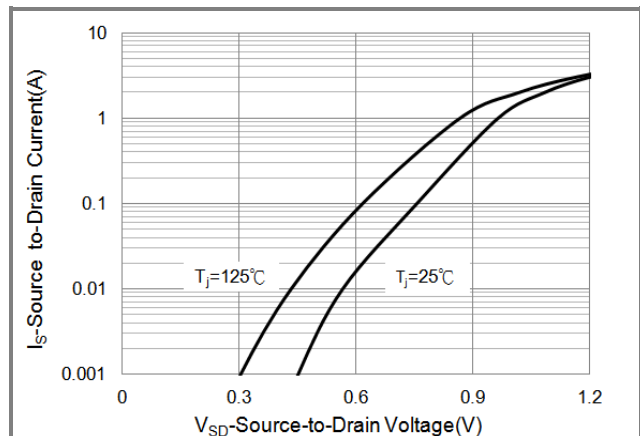


Fig.6 Body Diode Characteristics

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N-Channel TYPICAL CHARACTERISTIC CURVES

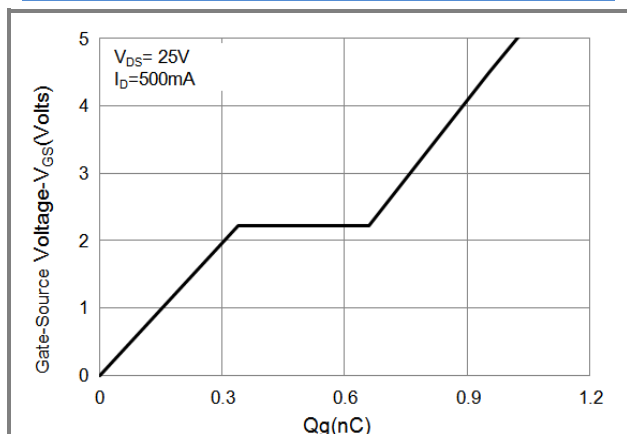


Fig.7 Gate-Charge Characteristics

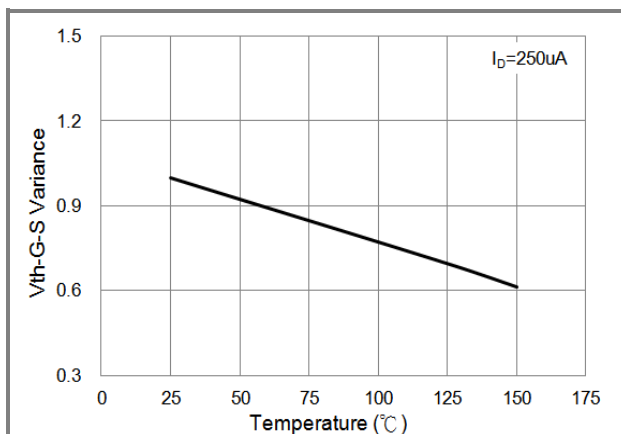


Fig.8 Threshold Voltage Variation with Temperature

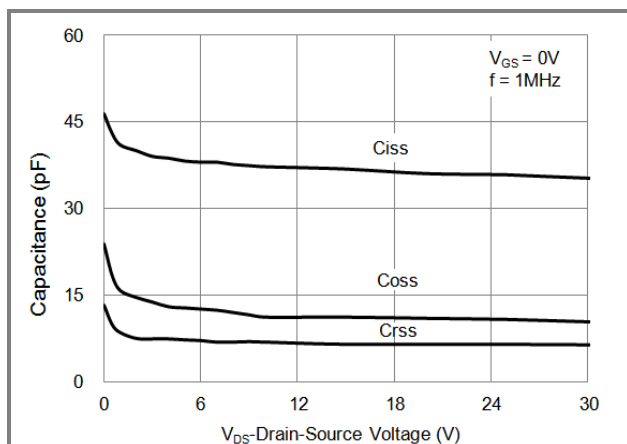


Fig.9 Capacitance vs. Drain-Source Voltage

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P-Channel TYPICAL CHARACTERISTIC CURVES

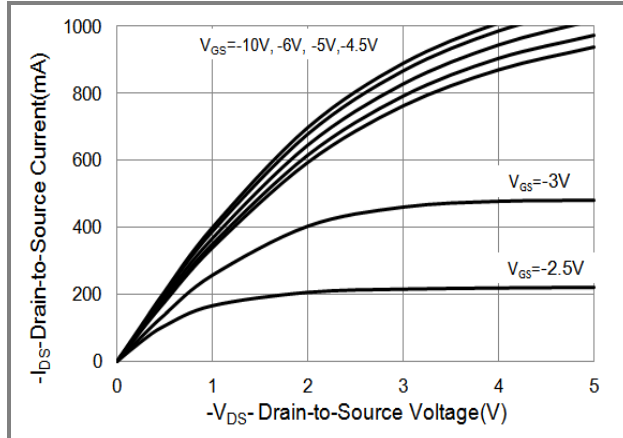


Fig.1 On-Region Characteristics

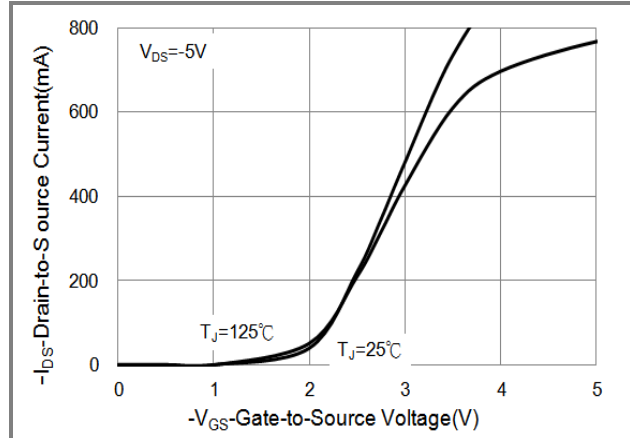


Fig.2 Transfer Characteristics

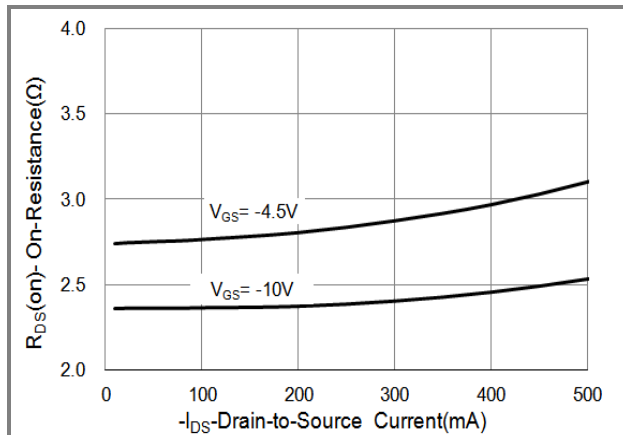


Fig.3 On-Resistance vs. Drain Current

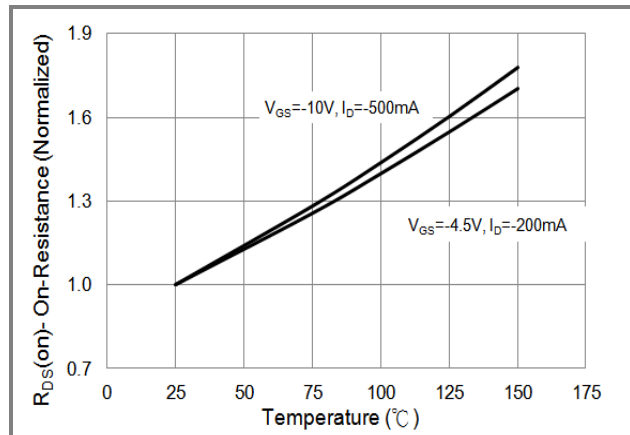


Fig.4 On-Resistance vs. Junction temperature

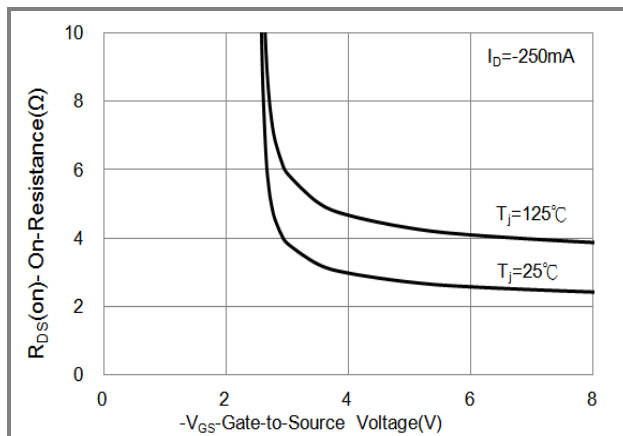


Fig.5 On-Resistance Variation with V_{GS}

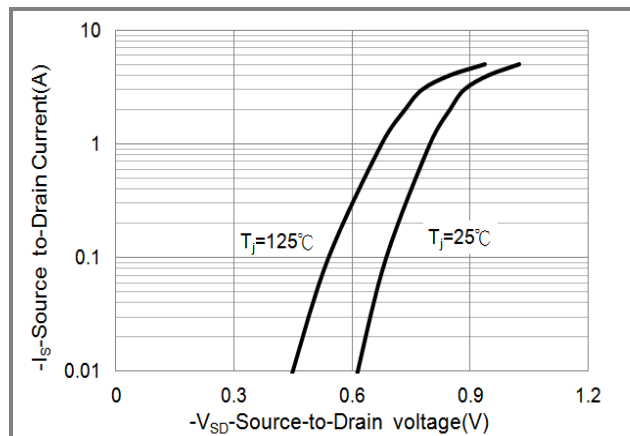


Fig.6 Body Diode Characteristics

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P-Channel TYPICAL CHARACTERISTIC CURVES

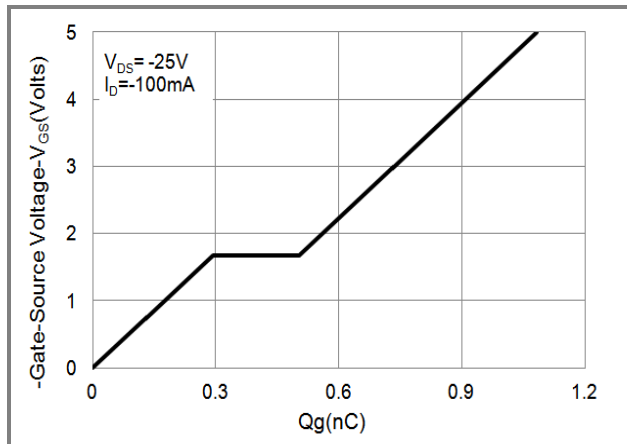


Fig.7 Gate-Charge Characteristics

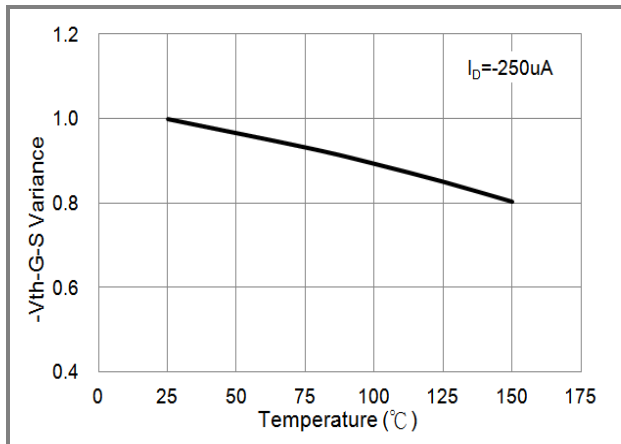


Fig.8 Threshold Voltage Variation with Temperature

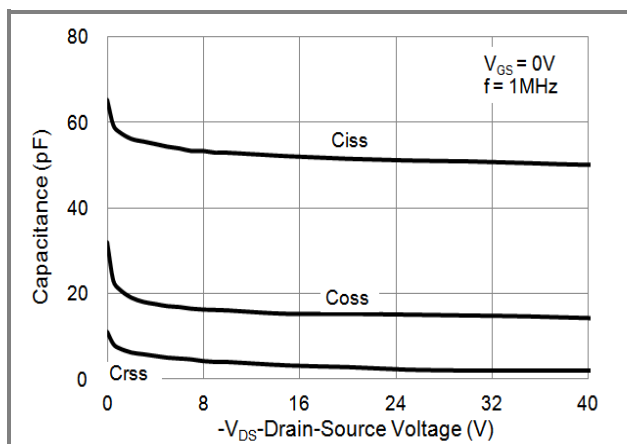


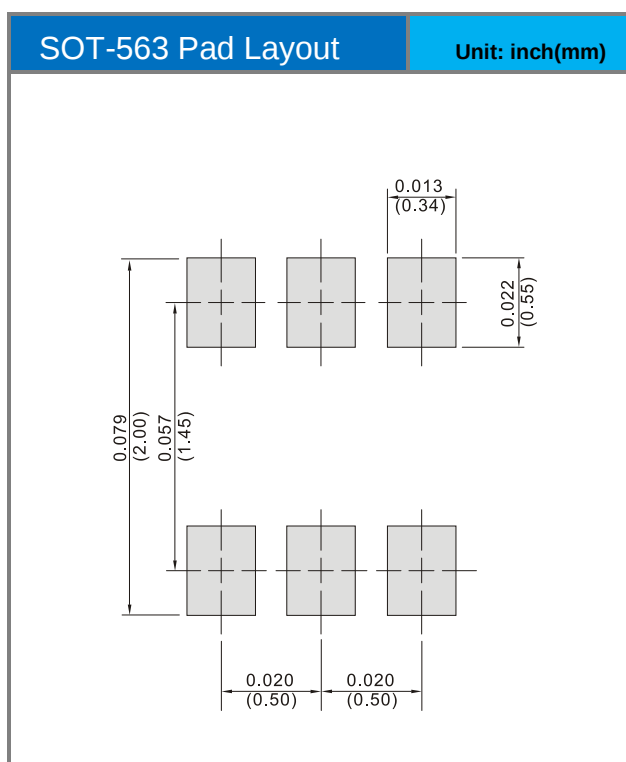
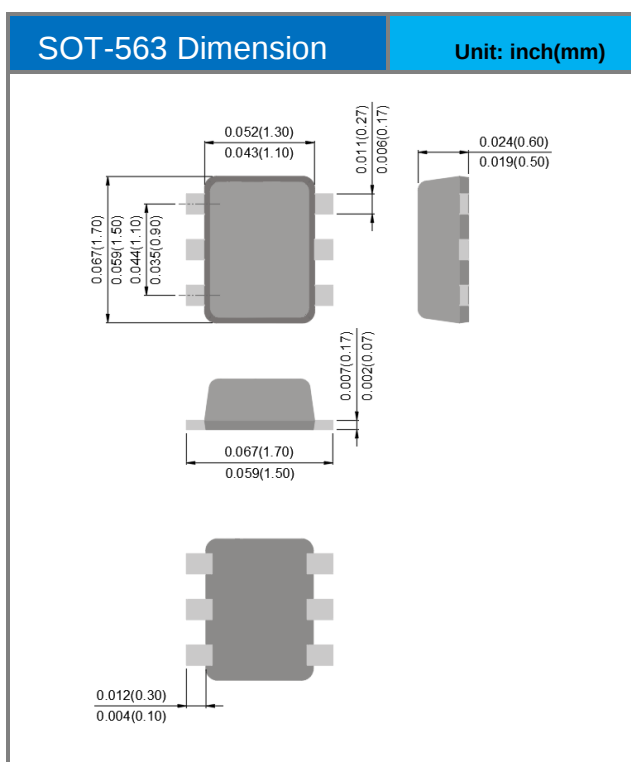
Fig.9 Threshold Voltage Variation with Temperature

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJX8603-AU	SOT-563	4K pcs / 7" reel	X63

Packaging Information & Mounting Pad Layout



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