

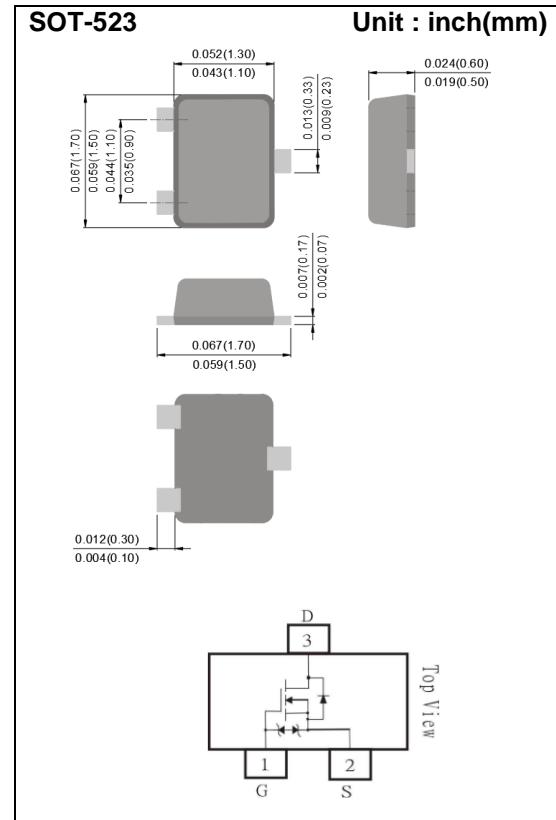
PJE138K

50V N-Channel Enhancement Mode MOSFET – ESD Protected

Voltage **50 V** **Current** **350mA**

Features

- RDS(ON) , VGS@10V, ID@500mA<1.6Ω
- RDS(ON) , VGS@4.5V, ID@200mA<2.5Ω
- RDS(ON) , VGS@2.5V, ID@100mA<4.5Ω
- Advanced Trench Process Technology
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard



Mechanical Data

- Case : SOT-523 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.002 grams

Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current		I_D	350	mA
Pulsed Drain Current		I_{DM}	1200	mA
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	223	mW
	Derate above 25°C		1.8	$\text{mW}/^\circ\text{C}$
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance - Junction to Ambient ^(Note 3)		$R_{\theta JA}$	560	$^\circ\text{C}/\text{W}$

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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	50	-	-	V
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.8	1.0	1.5	V
Drain-Source On-State Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=500\text{mA}$	-	0.96	1.6	Ω
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=200\text{mA}$	-	1.25	2.5	
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=100\text{mA}$	-	2.73	4.5	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}$	-	0.01	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	± 3.0	± 10	μA
Dynamic						
Total Gate Charge	Q_g	$V_{\text{DS}}=25\text{V}, I_{\text{D}}=250\text{mA}, V_{\text{GS}}=4.5\text{V}^{(\text{Note 1,2})}$	-	0.63	1	nC
Gate-Source Charge	Q_{gs}		-	0.2	-	
Gate-Drain Charge	Q_{gd}		-	0.23	-	
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, f=1.0\text{MHZ}$	-	25	50	pF
Output Capacitance	C_{oss}		-	9.5	20	
Reverse Transfer Capacitance	C_{rss}		-	2.1	5	
Switching						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=25\text{V}, I_{\text{D}}=500\text{mA}, V_{\text{GS}}=10\text{V}, R_{\text{G}}=6\Omega^{(\text{Note 1,2})}$	-	2.2	5	ns
Turn-On Rise Time	t_r		-	19.2	38	
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	6.2	12	
Turn-Off Fall Time	t_f		-	23	50	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	500	mA
Diode Forward Voltage	V_{SD}	$I_s=500\text{mA}, V_{\text{GS}}=0\text{V}$	-	0.86	1.5	V

NOTES:

1. Pulse width $\leq 300\text{us}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. R_{eJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper

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TYPICAL CHARACTERISTIC CURVES

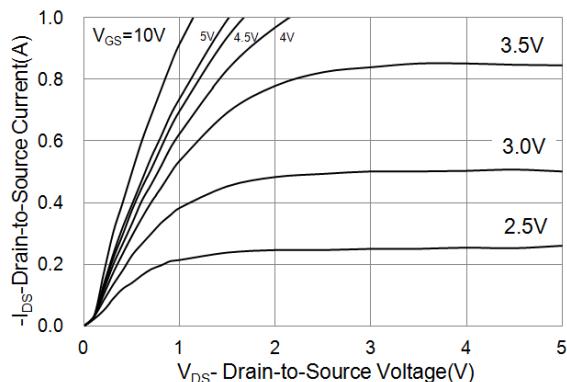


Fig.1 On-Region Characteristics

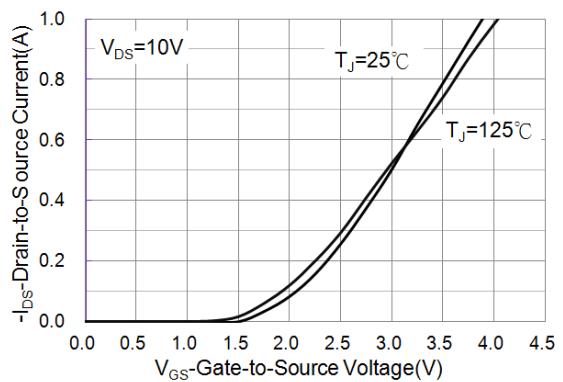


Fig.2 Transfer Characteristics

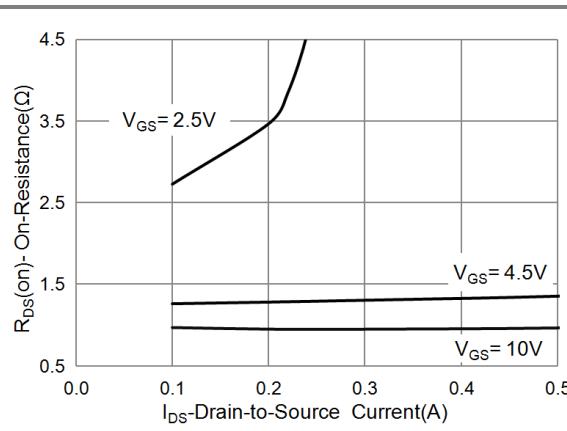


Fig.3 On-Resistance vs. Drain Current

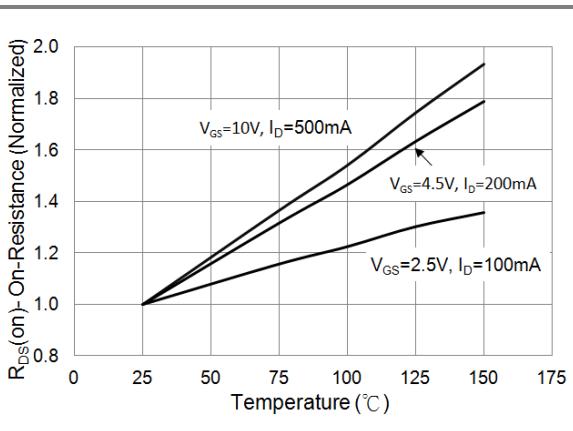


Fig.4 On-Resistance vs. Junction temperature

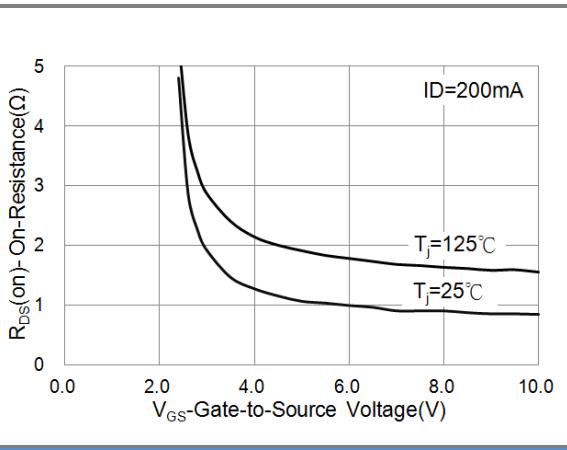


Fig.5 On-Resistance Variation with VGS.

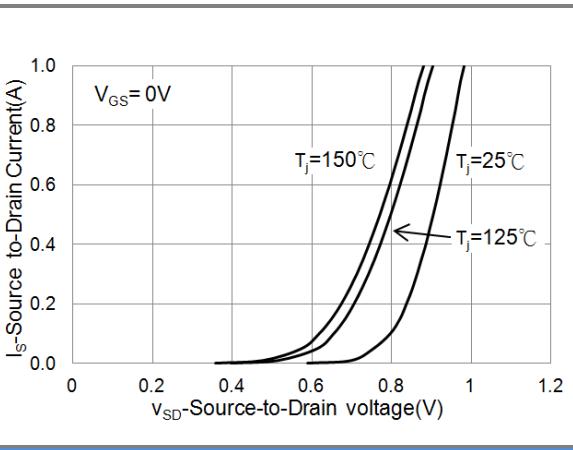


Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

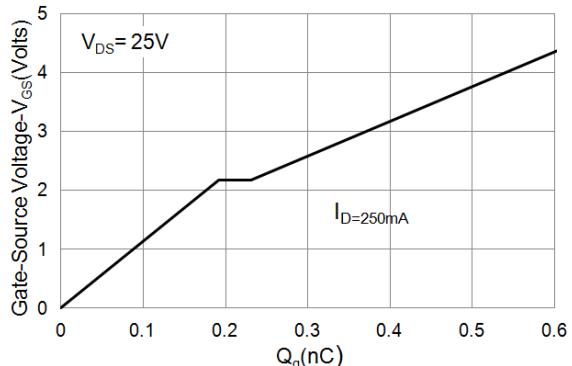


Fig.7 Gate-Charge Characteristics

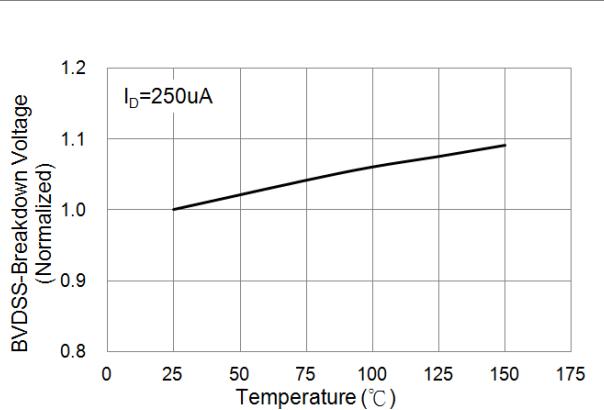


Fig.8 Breakdown Voltage Variation vs. Temperature

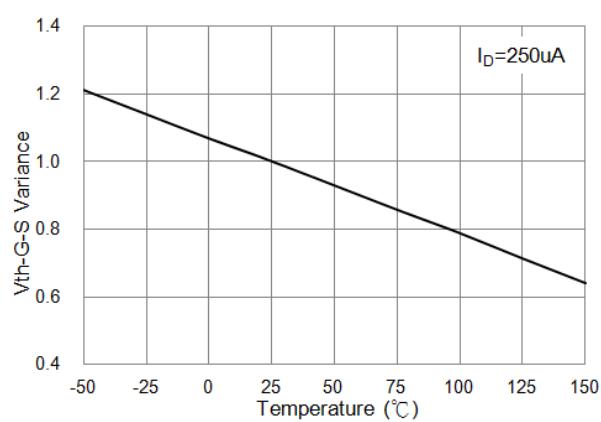


Fig.9 Threshold Voltage Variation with Temperature.

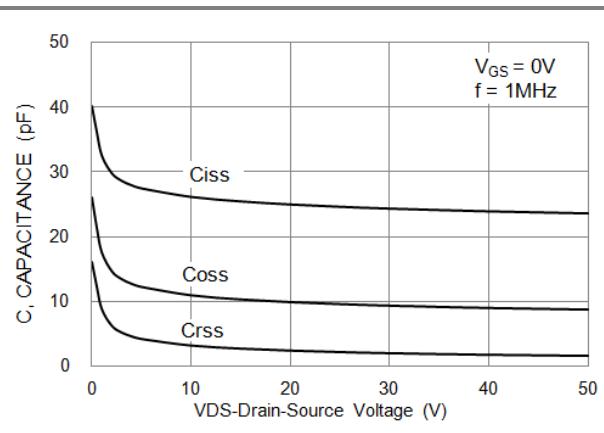


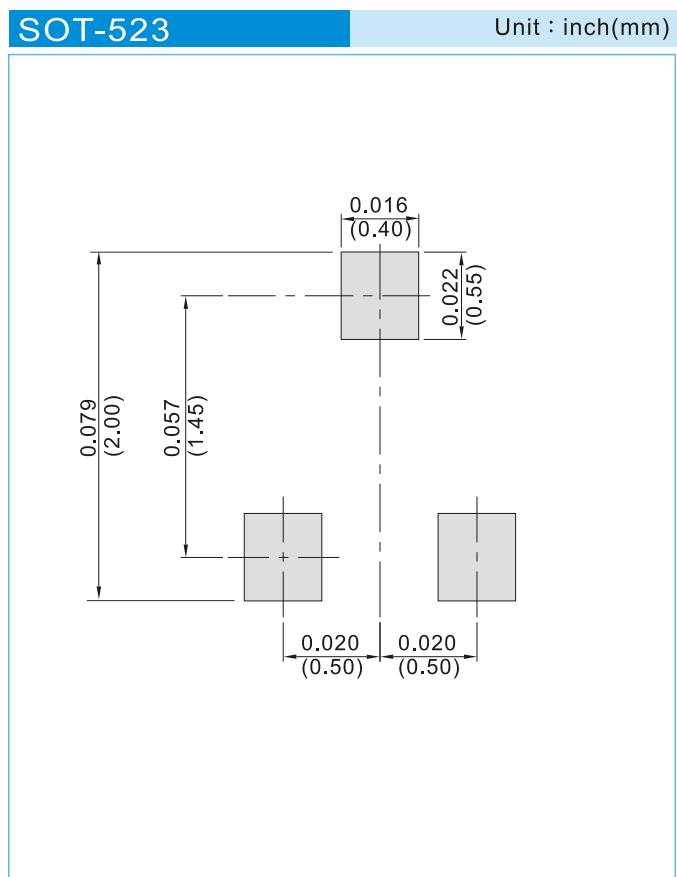
Fig.10 Capacitance vs. Drain-Source Voltage.

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJE138K	SOT-523	4K pcs / 7" reel	8KT

Mounting Pad Layout



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